Dual-Band Transmitters Using Digitally Predistorted Frequency Multipliers for Reconfigurable Radios

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Dual-Band Transmitters Using Digitally Predistorted Frequency Multipliers for Reconfigurable Radios

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CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

A/D	analog-to-digital
ACI	adjacent channel interference
ACPR	adjacent channel power ratio
ADC	analog-to-digital converter
ADS	advanced design system
AM	amplitude modulation
AMPS	advanced mobile phone service
ARB	arbitrary signal generator module
BJT	bipolar junction transistor
BPF	bandpass filter
CAD	computer aided design
CDMA	code division multiple access
CF	crest factor
CFR	crest factor reduction
D/A	digital-to-analog
dB	decibel
dBc	decibel compared to
DC	direct current
DHBT	double hetero-junction bipolar transistor
DQPSK	differential quadrature phase shift keying
DR	dynamic range
DSP	digital signal processing
EDGE	Enhanced Data rates for Global Evolution
ETSI	European Telecommunications Standards Institute
EVM	error vector magnitude
FET	field effect transistor
FM	frequency modulation
FSK	frequency shift keying
GaAs	gallium arsenide
GMSK	Gaussian minimum shift keying
GSM	global system for mobile communications
HEMT	high electron mobility transistor
HFET	hetero-structure field effect transistor
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IMD	intermodulation distortion
LAN	local area network
LMS	least mean square
LO	local oscillator
LPF	lowpass filter
LUT	look-up table

MESFET	metal-semiconductor field effect transistor
MSK	minimum shift keying
OFDM	orthogonal frequency division modulation
PA	power amplifier
PAE	power added efficiency
PAPR	peak-to-average power ratio
PCS	personal communication service
PD	predistortion
PM	phase modulation
PSK	phase shift keying
QAM	quadrature amplitude modulation
QPSK	quadrature phase shift keying
RF	radio frequency
RRC	root raised cosine
SDR	software defined radio
SPDT	single pole double throw
SRD	step recovery diode
WCDMA	wideband code division multiple access

SUMMARY

The objective of the proposed research is to develop simplified reconfigurable transmission systems with frequency multipliers for the transmission of complex modulated signals. Because they rely on nonlinear properties, frequency multiplier-based transmission systems require proper linearization techniques and accurate modeling of the signal transfer function. To accomplish these two goals, the author has developed techniques to model and linearize frequency multipliers and to digitize feedback signals for nonlinear characterization.

First, adaptive predistortion techniques and zonal transfer theories have been developed for modeling and linearization. The predistortion system has been verified by applying an IS-95B signal to various frequency multipliers built by the author.

Second, because the output signals at higher harmonic zones occupy wider frequency bandwidths than the signal in the fundamental zone does and thus make it harder to use traditional sampling techniques, a simplified but effective method called the sub-Nyquist sampling rate was developed and verified.

Third, two methods for reconfigurable transmitters using frequency multipliers in conjunction with digital predistortion linearizers were developed. Both methods make it possible to transmit complex signals via frequency multipliers by using dual-band transmission systems that incorporate frequency multipliers that are based on linearization techniques. One of these methods uses a circuit topology that can be switched between a fundamental-mode in-phase combined amplifier and a push-push frequency doubler using input phasing. The second suggested method uses a

fundamental-frequency power amplifier followed by a varactor multiplier that can be bypassed with an RF switch.

This work will contribute to the development of low-cost and size-effective reconfigurable transmission systems because it requires fewer transmitting components and needs less sampling of the feedback networks.

CHAPTER 1

INTRODUCTION

As frequency resources become crowded with various sources of radio transmissions, the requirements for higher frequency and higher spectral-efficient transmissions are increasingly more demanding. As such, the advent of various wireless standards in various frequency bands has led to the need to realize multiband or multistandard transceivers. Especially in the mobile communication industry, providing flexibility and mobility is essential for commercial products. In fact, to provide extended geographic coverage, commercially available mobile handsets are adopting software defined radio (SDR) techniques to accommodate multiple wireless standards. Although SDR is a promising technology for flexible all-purpose radios that can adopt different wireless standards via reprogramming, the major virtue of SDR is that it can give rise to a multimode configuration without the inclusion of separate hardware for each possible standard [1]. However, the failure to achieve fast analog-to-digital (A/D) and digital-to-analog (D/A) conversion processes from and to the radio frequency has been a bottleneck. For this reason, and because the different standards are often allocated different

frequency bands, most of today's multiband transceiver architectures are designed to switch their signal paths between two or three different bands as the mobile unit roams from one service area to another [2]. Fig. 1.1 shows the simplified architecture of a conventional dual-band transmitter.

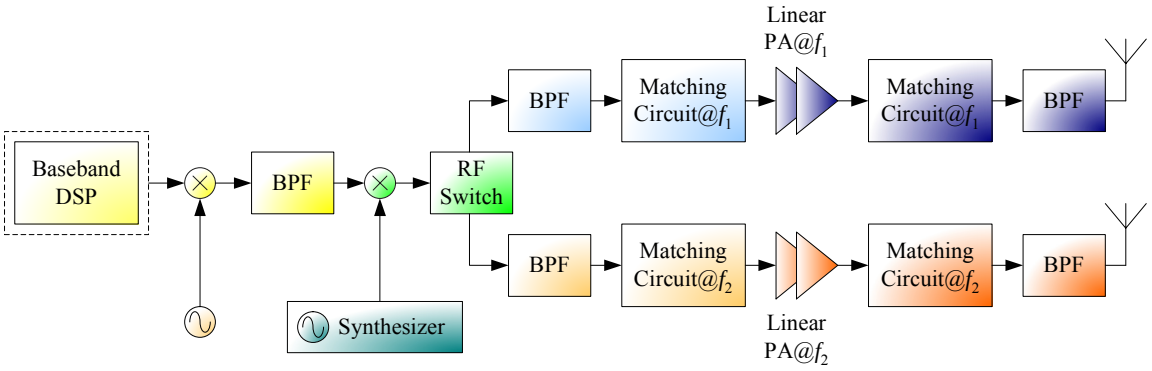


Fig. 1.1. Simplified block diagram of a conventional dual-band transmitter.

As a result, many components are duplicated because of the narrow bandwidths of most handset power-amplifiers (PAs). This duplication adds to system cost, physical board size, and weight. Thus, this increased system complexity has motivated researchers to look for alternative architectures that can transmit signals in two widely separated bands using reconfigurable, but nonredundant, front-end hardware. Single-chip transceiver and direct-conversion approaches are good examples of ways to eliminate or mitigate this overhead [3], [4]. However, the duplication of components in transceivers has not been resolved so far, and thus a new architecture that can eliminate this component redundancy in the dual-band transmission of bandpass signals is necessary.

A review of the evolution of communication technologies shows the steady widening of signal bandwidth since the first generation of mobile technology. This evolution can be represented by the changes between the advanced mobile phone system (AMPS), whose signal bandwidth was only 30 kHz, and the latest wireless LAN standard, IEEE802.11a, of 54 Mbps. These wideband signal transmissions place more stringent requirements on the hardware specifications, especially on the linearity of transmitters, which claim some linearization technologies [5]-[7].

When a signal passes through a nonlinear device, distortion typically occurs because of amplitude compression and phase deviation. In the case of PAs operating at the fundamental frequency, the major distortion contributors are AM/AM and AM/PM components that cause spectral regrowth in adjacent channels in the frequency domain and signal degradation [8]. The result is an increased error rate in the code domain. Furthermore, in a frequency multiplier that is strongly nonlinear by nature, far more AM/AM and AM/PM distortion, along with additional PM/AM and PM/PM, is introduced into the envelope signal as well as into the carrier frequency to be multiplied [9]. Therefore, a linearization technique is mandatory for the transmission of complex signals through a frequency multiplier; however, the need for this linearization is not a function of the PM/AM distortion, which can be ignored because it is relatively small in proportion to the magnitude of the other types of distortion.

The second problem in terms of the sampling requirement of an A/D conversion process is that in the feedback network of a linearization system, even if signals at the RF could be downconverted, the sampling frequency must be twice the maximum frequency component of the signal that is to be received. This condition is expected to become

more stringent because the bandwidths of the latest standards tend to be wider. Furthermore, for a transmitter that adopts a digital linearization technique, this Nyquist sampling requirement is even harder to meet because the bandwidth of a distorted signal will be at least three times the bandwidth of the original signal. This will necessitate a sampling frequency six times the maximum frequency of the original signal [10]. Consequently, a technique to mitigate the full Nyquist-rate sampling requirement is needed for a simplified, low-cost hardware transceiver.

1.1 DUAL-BAND SIGNAL TRANSMITTERS

To meet the reconfigurability demand stated above, new dual-band signal transmission architectures are introduced: They employ an amplifier for the fundamental frequency operation and they can be switched to frequency multipliers as frequency conversion devices. Fig. 1.2 represents the idea.

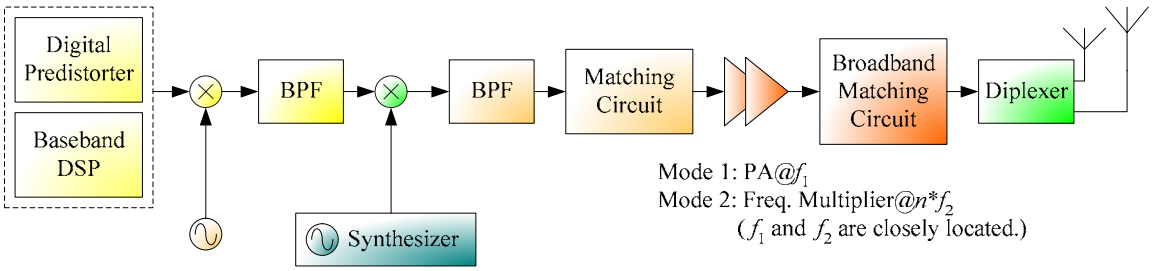


Fig. 1.2. Simplified block diagram of suggested architecture for dual-band transmitters.

The first step toward proving the feasibility of the architecture demonstrates that it is possible to apply advanced predistortion methods to frequency multipliers to transmit digitally modulated signals without excessive adjacent channel interference (ACI) [11], [12]. In the second step, dual-mode transmitters are introduced by two dual-band reconfigurable transmitter architectures [13], [14]. The first architecture uses a PA with mode-switching capability that can reconfigure from an in-phase PA in the fundamental mode to a push-push frequency doubler in the second harmonic mode. In addition, an innovative output combiner named 'bi-tuned combiner' had to be designed to satisfy different optimum output load-line conditions for maximum output power at the fundamental frequency in the amplifier mode and at the second harmonic in the doubler mode. The switching between modes can be done by using a control signal to change the phase angle of one of the signal paths. The second architecture uses a passive, low-loss varactor frequency doubler after a fundamental mode PA to achieve the second harmonic transmission; this doubler can be bypassed by an RF switch to transmit signals into the fundamental frequency.

RF IC technology could be used to optimize the architectures of both the active and passive reconfigurable dual-band transmitter architectures described here. However, to validate the concepts involved, the author has used commercially available components to construct prototypes on printed circuit boards. The essential building blocks for the architectures have been validated, and their performance is reported herein.

1.2 DIGITAL PREDISTORTION WITH SUB-NYQUIST RATE FEEDBACK

One popular linearization technique is baseband digital predistortion in which a device's nonlinearity is characterized and its inverse function is generated in the digital domain. In recent years, great improvements in the performance and processing costs of digital signal processing (DSP) chips have made it feasible to implement baseband predistorters for signal transmission with relatively lower cost and less complexity while retaining comparable performance with feedforward and feedback techniques [10]. Meanwhile, because adaptive predistortion systems require feedback networks to track the characteristic drifts that occur over time, an A/D conversion process is needed to gather information from the input and output signals of the device. However, as signal bandwidths become wider, the spectral regrowth of the signal at the output of the nonlinear device makes it is harder to fulfill the sampling requirements at the feedback network of predistorters with the A/D converters that are currently available. Moreover, the higher sampling rate necessitates more storage space and computing power for the sampled data, both of which relate directly to the cost of the system. These technical challenges and economics have given rise to alternative sampling methodologies that require lower sampling rates. These alternative sampling technologies take advantage of the reciprocity of the signal spectrum in the frequency domain [15]-[17]. Further research shows that for Volterra nonlinear systems, the sampling rate of the output signal is sufficient when it is twice the maximum frequency component of the input signal, whereas at this rate the output signal is aliased with its images [18]. This subsampling or sub-Nyquist rate sampling, as this technique is termed, is being suggested and verified in this thesis for use in the feedback networks of adaptive predistortion systems.

1.3 OUTLINE OF THE THESIS

The rest of this dissertation is organized as follows. Chapter 2 introduces theories of frequency multipliers and linearization techniques. By introducing these fundamental theories and undertaking brief surveys of the classification and the characteristics of frequency multipliers, the possibility of using these devices as frequency converters for digital signals is examined. Subsequently, the effects of nonlinear distortion on the magnitude and phase of a transmitted signal are identified, and digital predistortion techniques to linearize nonlinear devices are explained. In addition, the next section introduces a crest-factor reduction (CFR) technique, which effectively reduces the dynamic range of the input signal, as a supplementary method to reduce distortion.

Chapter 3 covers the feasibility of transmitting complex signals through frequency multipliers. The nonlinear transfer function of frequency multipliers is developed after the introductory section, and the next two sections describe the predistortion-system setup and the experimental results.

Chapter 4 introduces two ideas of using dual-mode frequency doublers to complete dual-band transmission systems with frequency multipliers. The first three sections show the concepts of two dual-mode frequency doublers, and Section 4.4 explains the application of digital predistortion to these frequency doublers.

Chapter 5 combines the proven feasibility of the predistortion of frequency multipliers from Chapter 3 and sub-Nyquist rate sampling theory to accommodate further simplified transmission system architectures. After the description of the sub-Nyquist rate sampling idea and its related sampling theories in Section 5.1 and 5.2, the adaptive predistortion systems adopted for the linearization of PAs and frequency multipliers are

explained, and finally the predistortion performances with sub-Nyquist sampling rates are discussed.

Finally, we conclude this thesis with a summary of the work it covers and a statement of the key contributions of this work.

Fig. 1.3 illustrates the adaptive digital predistortion system for a dual-mode transmitter. The bolded block in the figure represents the dissertation content that will be covered here.

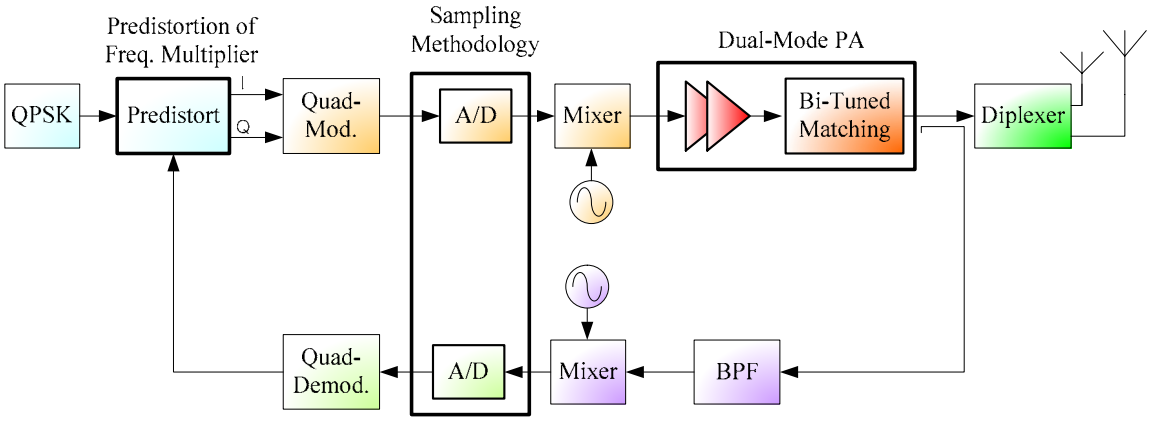


Fig. 1.3. Overview of dissertation content.

CHAPTER 2

FREQUENCY MULTIPLIERS AND NONLINEAR DISTORTION

2.1 INTRODUCTION

Nonlinearity within a device such as PA distorts the transmitted signal and causes it to spread outside its bandwidth and to generate unwanted harmonics of the carrier frequency. When the amplifiers have the same operation frequency at the input and output terminals, this nonlinearity causes interference with other signals and a loss of efficiency. For these reasons, considerable research has been undertaken to minimize this nonlinearity in PAs by means of backing off the operating point and employing various linearization techniques [5]-[7], [10].

However, from the perspective of frequency multipliers, such nonlinearity does not present a problem. This is because nonlinearity is an essential property for harmonic generation and consequently devices showing higher nonlinearity in resistance, capacitance, or transconductance are considered good frequency multipliers [19], [20].

Nevertheless, although frequency multiplication is based on the nonlinearity of the devices, proper linearization should be applied to the modulated bandpass signal — not to the carrier signal — so that the signal at a harmonic of the input carrier frequency can be received successfully with reasonably low distortion.

In any case, it is necessary to examine the properties of frequency multipliers and also the properties of the distortion generated from any nonlinear devices.

2.2 FREQUENCY MULTIPLIERS AND THEIR APPLICATIONS

Frequency multiplication is a well-known technique for generating high-frequency local-oscillator signals [21]. This technique is preferred when a low phase noise signal at high frequency is required but is beyond the practical range of fundamental mode oscillators and phase-locked loops. Generally, harmonic generation is done by using the nonlinear characteristics of components such as varactor diodes, step-recovery diodes (SRDs), and Schottky-barrier diodes [22], [23]. Varactor multipliers, often classified along with SRD multipliers as reactive multipliers, rely on a nonlinear $C(V)$ characteristic, and they are usually employed when very low noise multiplication is desired, such as multiplication orders of three to five. However, they have a relatively higher conversion loss for high harmonic generation and are generally narrowband; SRDs are used for high harmonic generation because of their abrupt reverse recovery properties; their primary disadvantage is also the narrow bandwidth of operation. Resistive multipliers, represented by Schottky multipliers, generate harmonics by the exponential behavior of the I-V characteristics and are often restricted to multiplication factors of no more than three [24].

However, because they are inherently broadband, Schottky multipliers have significant advantages over reactive multipliers or SRDs. Lastly, active components such as FET, MESFET, and HEMT devices have exponential I-V characteristics, and thus they are also used as frequency multipliers to achieve conversion gains [21], [25]-[27]. Table 1 shows the classification of frequency multipliers and their characteristics.

Table 1. Classification of frequency multipliers and their characteristics.

Multiplier Type	Characteristics	Typical Applications
Single-diode resistive doubler	Simple, narrowband, ≅ 10dB loss.	Low-cost, low performance applications.
Anti-parallel diode tripler (Odd-order, resistive)	Broadband, low efficiency. Conversion loss is 13~16dB.	Applications for wideband but where high conversion loss is tolerable.
Varactor frequency doubler	Narrowband, relatively unstable. Conversion loss is 3~5dB. Low noise.	Mixer LO.
Step-recovery diode multiplier	Best in high-order frequency multiplication.	Mixer LO, frequency synthesizer.
Single-device active frequency multiplier	Good efficiency and moderate bandwidth. Fundamental frequency leakage.	Where general design is needed, like in small-size IC designs.
Balanced active doubler	Low fundamental frequency leakage. Optimum load impedance is easier to realize.	Most doublers adopt this circuit.

2.2.1 Resistive Frequency Multipliers

As for passive frequency multipliers, equation (2.1) shows the current through a Schottky-diode as a function of the applied voltage $V(t)$.

$$I(x) = I_s\left[\exp(x) - 1\right], \tag{2.1}$$

where

$$\begin{aligned} x &= qV(t)/kT_a \\ q &= \text{electron charge} \\ k &= \text{Boltzman constant} \\ T_a &= \text{absolute temperature} \\ I_s &= \text{diode saturation current.} \end{aligned}$$

By applying the Fourier series expansion to this equation, we can see the frequency components that multipliers count on for harmonic generation.

$$I(x) = I_s\left[I_o(x) + 2\sum_{1}^{\infty} I_n(x)\cos(n\omega t) \right], \tag{2.2}$$

where $I_n(x)$ is the modified Bessel function of the first kind, which determines the level of the harmonic components. Since the modified Bessel function has lower values with higher orders, and the difference between orders of the function is higher when x is small, this equation shows that the conversion loss is worse at low input voltages and gets better with higher input voltages. However, as the input is increased further, the diode current reaches its saturation current and its harmonic components saturate as well.

A simple frequency multiplier can be built by connecting a pair of diodes in parallel. Depending on the intended order of frequency multiplication, input and output circuits must have proper matching circuits that should be seen as open circuits at desired frequencies and as short at all other harmonics. An example of an odd-order diode frequency multiplier is shown in Fig. 2.1. The circuit can be configured as an even-order multiplier by changing the way the diode current is combined at the output load.

Anti-phase combining of parallel diodes cancels odd harmonics, and in-phase combining of anti-parallel diodes cancels even terms. For each case, the current through the load Z_L is represented as below [21]:

$$I_{total} = 2I_s\left[I_o(x) - 1 + 2\sum_{1}^{\infty} I_n(x)\cos(2n\omega t)\right]: \quad \text{Even order multiplier, (2.3)}$$

$$I_{total} = 4I_s\left\{\sum_{1}^{\infty} I_{2n+1}(x)\cos\left[(2n+1)\omega t\right]\right\}: \quad \text{Odd order multiplier. (2.4)}$$

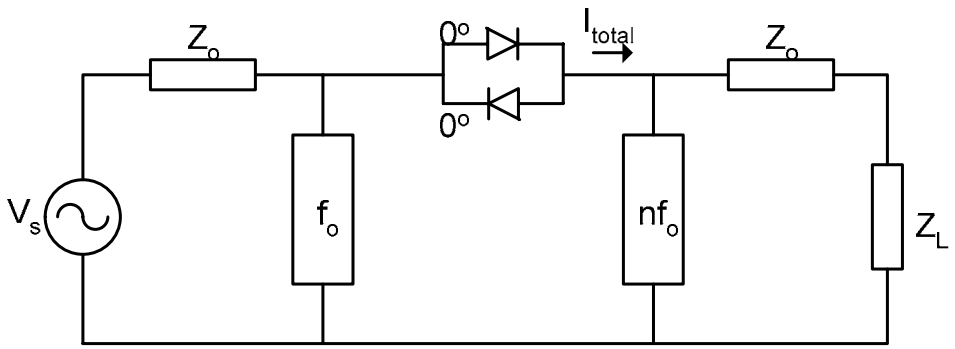


Fig. 2.1. Circuit diagram of an odd-order frequency multiplier.

Because this type of resistive frequency multipliers mainly rely on the nonlinear I-V characteristics, resistive frequency multipliers are naturally broadband and stable, even though they have poor conversion losses, $1/n^2$ at best, where n is the harmonic number [24]. To minimize the poor efficiency of resistive frequency multipliers, computer-aided design (CAD) tools with optimization functions are employed [23]. Another way to

mitigate the conversion loss problem is to adopt balanced topologies, although baluns limit the bandwidth of the multipliers. Mass introduced a broadband balun in an effort to overcome the limited bandwidth issues in baluns [22].

2.2.2 Reactive frequency multipliers

The characteristics of reactive frequency multipliers are the opposites of resistive ones: higher efficiency, and lower noise. Because of the strong nonlinearity in SRDs that form the majority of the reactive frequency multipliers, the analysis of the reactive frequency multipliers with SRDs has mainly been based on Hamilton and Hall's method [28], which assumes an SRD is an ideal diode and an ideal capacitor, assumptions that lead to inaccuracies in practical applications. With increasing demand for integrated circuits in which any circuit modification is costly, accuracy in design is essential. Zhang suggested an accurate model for SRDs and showed an efficient model for simulation that retains accuracy [23], [29].

2.2.3 Active Frequency Multipliers

Active frequency multipliers are attracting a lot of attention as an alternative to gain more signal power at a desired frequency and as a way to implement frequency multipliers in ICs; the major contributing elements of active transistors to nonlinear behavior are drain-source current I_{ds}, gate-source capacitance C_{gs}, and gate-drain capacitance C_{gd} [30]-[40]. In terms of design issues for active frequency multipliers, the choice of the bias point is critical for the efficiency and performance of the devices.

Therefore, in an effort to analyze performance regarding the biasing of active devices, O'Ciardha *et al.* presented a generalized method to assess the performance of frequency multipliers [30]. In terms of harmonic numbers, Filipovic designed an x7 frequency multiplier using a double hetero-junction bipolar transistor (DHBT) [36], but most research has focused on low-order harmonic generations between two and four. Other than that, the majority of the work has been on implementing active frequency multipliers on various transistor technologies [32]-[35], [37]. Fig. 1.1 shows the comparison of recently published active frequency multipliers with respect to output frequency and the harmonic number. The conversion losses or gains are also expressed in this figure.

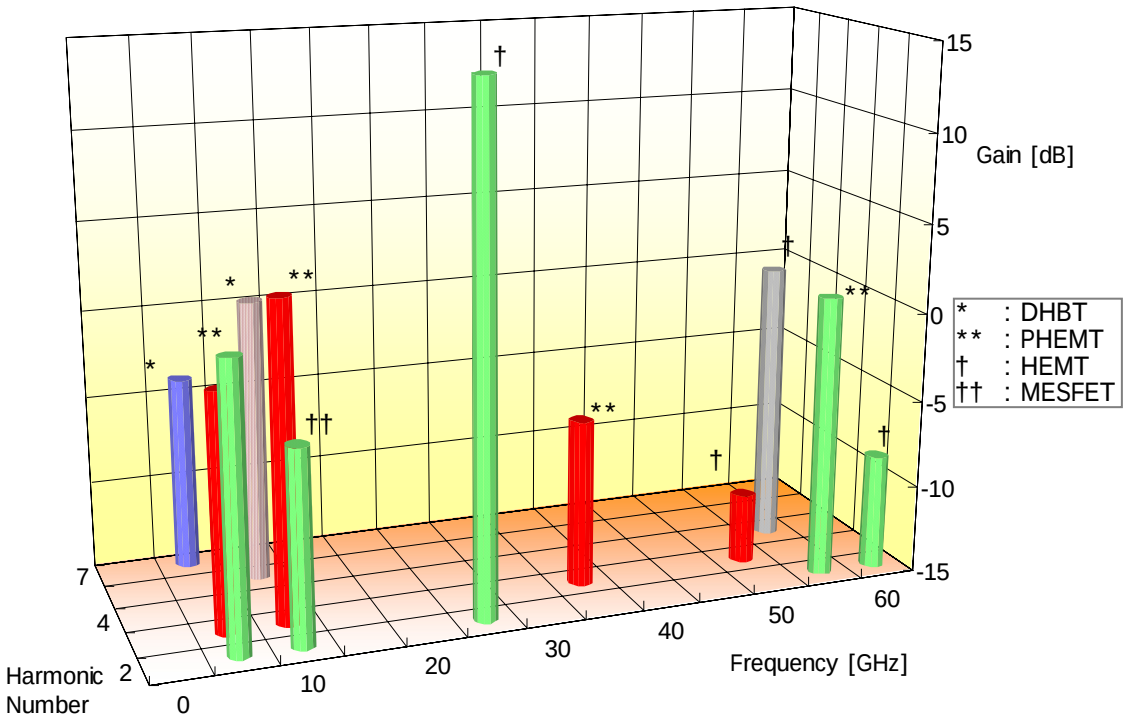


Fig. 2.2. Comparison of active frequency multipliers.

2.2.4 Applications of Frequency Multipliers

Traditional RF or microwave communication systems for digital modulated signals contain several stages after the intermediate frequency (IF), including an upconverting mixer, a local generator, and some image rejection filters. Thus, much research has been done on replacing these costly components with a simple frequency-converting component. A frequency multiplier is one of the strongest candidates for this purpose. However, because of the highly nonlinear distortion used to generate harmonics, phase modulation (PM) undergoes a linear multiplication by the same order as the frequency multiplication, and any amplitude modulation (AM) existing in the signal is also highly distorted. For these reasons, transmitting modulated signals without mixers has been limited to continuous-envelope modulations. As such, constant envelope modulations, such as PM or frequency modulation (FM) may be used in conjunction with frequency multipliers with a linear scaling in modulation index, but there is no way to compensate for the nonlinear distortion of the baseband envelope. In particular, based on the idea that MSK modulation is equivalent to continuous phase FSK with a modulation index of one half, Kumar showed that with the proper devices to manipulate the frequency and phase, the MSK signal could be directly modulated into the microwave frequency [41], [42]. Similarly, Klymyshyn *et al.* applied a Gaussian minimum shift keying (GMSK) modulated signal to a frequency multiplier with improvements in the simplicity of the system, leading to a suitable solution for microwave monolithic IC implementation [43]. However, as stated above, the highly nonlinear nature of frequency multipliers has precluded the use of AM in direct modulation.

2.3 DISTORTION OF NONLINEAR DEVICES AND LINEARIZATION TECHNIQUES

2.3.1 Nonlinear Distortion

Amplitude distortion refers to any distortion occurring in $m(t)$ except for the linear multiplication by a factor when an amplitude and phase modulated signal can be expressed as

$$v(t) = m(t)e^{j(\omega_c t + \phi(t))}, \tag{2.5}$$

where ω_c is carrier frequency, $m(t)$ is amplitude modulation, and $\phi(t)$ is phase modulation. That is, a perfectly linear device would have a linear amplitude transfer function as shown below.

$$v_{out}(t) = c_1 \cdot v(t), \tag{2.6}$$

where the scalar constant c_1 is called the gain or loss of the device.

For an amplitude transfer characteristic that has any other components than the linear scalar, the output voltage can be expressed with additional higher order terms as

$$\begin{aligned} v_{out}(t) &= c_1 \cdot v(t) + c_2 \cdot v^2(t) + c_3 \cdot v^3(t) + \cdots \\ &= \sum_{k=1}^{P} c_k \cdot v^k(t) \end{aligned}, \tag{2.7}$$

where the coefficient c_k is a complex number. The high order terms in (2.7) cause harmonic distortion from single frequency components and intermodulation distortion from the interaction of each different frequency component. Rewriting (2.7) by the

amplitude and the phase of the output signal as in (2.5), we can derive the amplitude and phase components as functions of the amplitude and phase of the input signal.

$$\begin{aligned} v_{out}(t) &= m_{out}(t)e^{j\phi_{out}(t)} \\ &= F_{AMAM}(m(t)) \cdot F_{PMAM}(\phi(t)) \cdot e^{j \cdot G_{AMPM}(m(t)) \cdot G_{PMPM}(\phi(t))}, \end{aligned} \tag{2.8}$$

where $F_{AMAM}(\cdot)$, $F_{PMAM}(\cdot)$ are amplitude distortion; $G_{AMPM}(\cdot)$, $G_{PMPM}(\cdot)$ are phase distortion.

In a case in which all $F(\cdot)$ and $G(\cdot)$ are functions of only the current instant t, a system is classified as memoryless. Such a memoryless classification is generally assumed in this thesis. On the other hand, when all $F(\cdot)$ and $G(\cdot)$ have inputs from the past, the system is called a system with memory, and the reasons for this memory are presumed to be the device's self-heating, improper termination at the envelope frequency, and nonlinear parasitic reactance either as individual causes, combinations of two or more circumstances or all three simultaneously [10], [44].

As the $F_{AMAM}(\cdot)$ has the $m(t)$ as its own input, it is called AM/AM distortion, meaning that the output magnitude is distorted by the input magnitude. Similarly, $F_{PMAM}(\cdot)$, $G_{AMPM}(\cdot)$, and $G_{PMPM}(\cdot)$ are called PM/AM, AM/PM, and PM/PM distortion, respectively. In the case of devices such as amplifiers that are operating in the fundamental harmonic zone, PM/AM and PM/PM are negligible compared with the distortion caused by AM/AM, AM/PM, or memory effect, whereas it is considered more accurate to include these effects in modeling IQ modulators [45]. In addition, in the distortion analysis of frequency multipliers, PM/PM has been shown to be an important distorting factor [12], [46]. The in-band distortion resulting from these nonlinear properties can be visualized by the comparison of constellations of signals. Fig. 2.3 represents the results of AM/AM,

AM/PM, PM/AM, and PM/PM distortion to the 64-quadrature amplitude modulation (QAM) input signal. As shown in these pictures, the in-band distortion is acting as noise and deteriorating the quality of the signal.

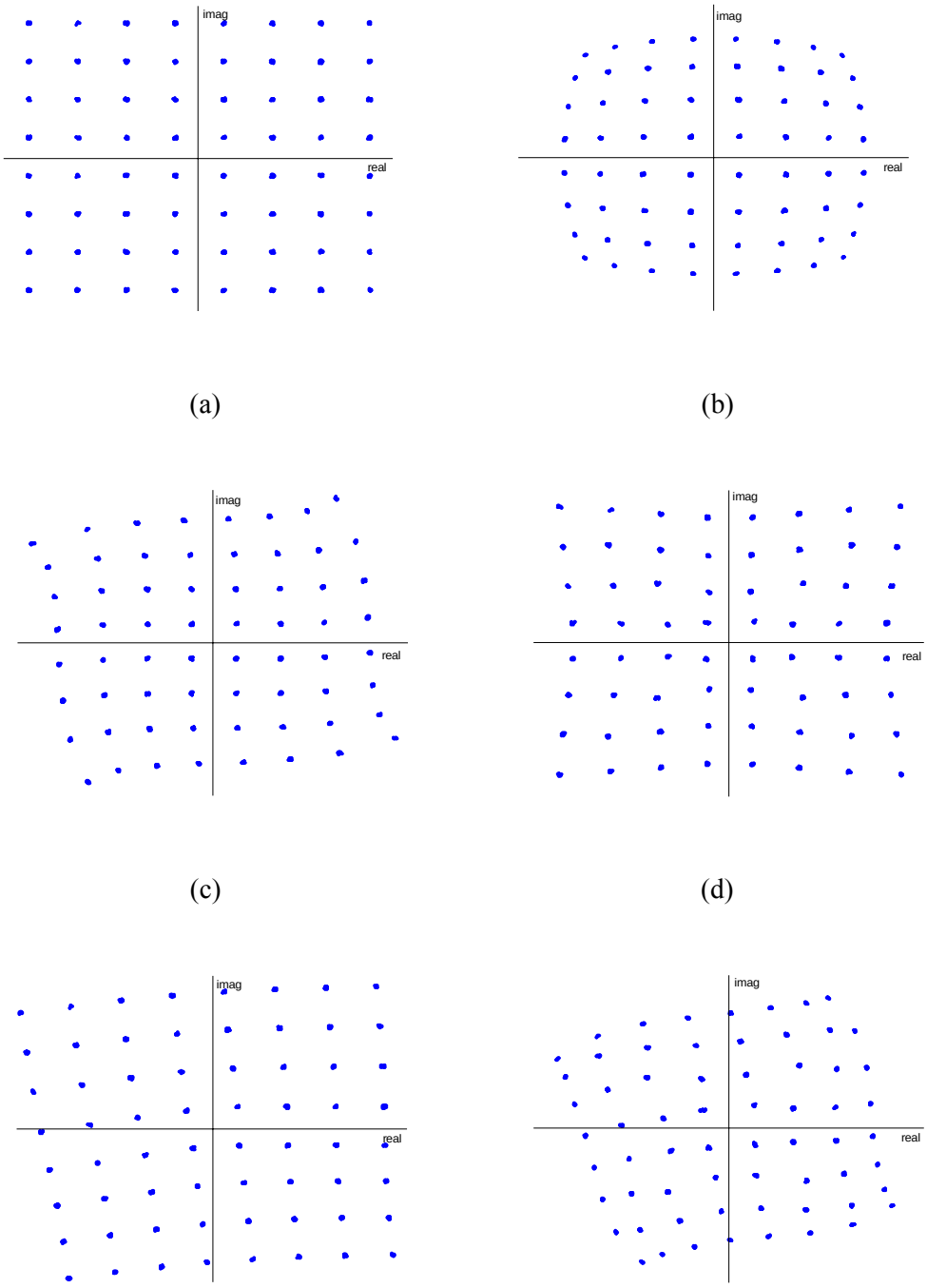


Fig. 2.3. Constellation degradation from nonlinear distortion: (a) distortion free 64-QAM (b) AM/AM (c) AM/PM (d) PM/AM (e) PM/PM (f) all effects combined.

The effect of distortion from a nonlinear device in the frequency domain can be assessed by applying a two-tone signal. In the two-tone test, the harmonic distortion results in multiples of each tone, whereas the intermodulation distortion generates additional tones at all possible combinations of two frequencies.

The two-tone signal with frequencies at ω_1 and ω_2 can be defined as

$$\begin{aligned} v(t) &= \cos(\omega_1 t) + \cos(\omega_2 t) \\ &= \cos((\omega_c - \omega_d)t) + \cos((\omega_c + \omega_d)t), \end{aligned} \tag{2.9}$$

where ω_c is the center frequency, and ω_d is the modulation frequency between ω_1 and ω_2.

Then, using the definition of a complex envelope signal [47], (2.9) can be rewritten as

$$\begin{aligned} v(t) &= \mathrm{Re}\left[v_c(t) \cdot e^{j \cdot \omega_c t}\right] \\ &= \frac{1}{2}\left[v_c(t) \cdot e^{j \cdot \omega_c t} + v_c^{*}(t) \cdot e^{-j \cdot \omega_c t}\right], \end{aligned} \tag{2.10}$$

where $v_c(t) = e^{j\omega_d t} + e^{-j\omega_d t}$.

Expanding the polynomial equation of (2.7) by (2.10), the output signal from the n^{th} order nonlinearity is shown as

$$v^n(t) = \frac{1}{2^n} \sum_{k=0}^{n} \binom{n}{k} v_c{}^k(t) \cdot \left[v_c^{*}(t)\right]^{n-k} \cdot e^{j \cdot \omega_c (2k-n)t}. \tag{2.11}$$

When only amplitude distortion is considered, the input two-tone signal of frequencies ω_1 and ω_2 introduces harmonics and intermodulation distortions inside and outside of the desired band. Table 2 shows the list of frequency components with amplitudes when two tones are applied to the system with nonlinearity of up to the 4th order. From this table, we can clearly see that the response of the n^{th} zone is composed of not only the n^{th}

order nonlinearity but also of higher order nonlinearities, which means that the n^{th} order power does not always show the exact n:1 input-output power relation in dB scale [10], [12].

In the case of amplifiers, because only the fundamental zone signal is of interest and also because of the simplicity of simulation and calculation, most of the modeling effort for amplifiers focuses on the odd order distortion in the fundamental zone, although there exists the possibility that even-order nonlinearities affect odd-order distortion [10]. In contrast, with frequency multipliers, the desired harmonic number for the output signal determines the order of main interest.

Table 2. Distortion products and their amplitudes classified by zones.

		$v(t)$	$v^2(t)$	$v^3(t)$	$v^4(t)$
DC Zone	DC		1		9/4
	2ωd		1		3
	4ωd				3/4
1st Zone	ωc - 3ωd			3/4	
	ωc - ωd	1		9/4	
	ωc + ωd	1		9/4	
	ωc + 3ωd			3/4	
2nd Zone	2ωc - 4ωd				1/2
	2ωc - 2ωd		1/2		2
	2ωc		1		3
	2ωc + 2ωd		1/2		2
	2ωc + 4ωd				1/2
3rd Zone	3ωc - 3ωd			1/4	
	3ωc - ωd			3/4	
	3ωc + ωd			3/4	
	3ωc + 3ωd			1/4	
4th Zone	4ωc - 4ωd				1/8
	4ωc - 2ωd				1/2
	4ωc				3/4
	4ωc + 2ωd				1/2
	4ωc + 4ωd				1/8

2.3.2 Predistortion Linearization

Predistortion linearization is a known technique for reducing distortion in RF power amplifiers (PAs) [6], [10], and it involves modifying the device input signal to counteract the signal distortion that arises from gain compression (AM/AM distortion) and phase deviation (AM/PM distortion). Analog approaches using simple Schottky diodes or passive FET have shown competitive results in terms of cost effectiveness; however, the main drawbacks of such a solution have been the limited order of nonlinearity cancellation, a lack of precision, and the lack as well of adaptability because of the open-loop correction [48], [49]. Recently, because of its renewed performance in DSP and analog-to-digital converter (ADC), digital predistortion has been in the spotlight of research and development. Given accurate nonlinear device models, the generation of inversely nonlinear functions is done most precisely by using DSP in mathematical operations on the baseband signals. Moreover, if a feedback path is incorporated, the use of digital techniques allows the system to adapt to changes in voltage, temperature, and other environmental factors. In the usual architecture, the predistorted signals are converted to analog form, upconverted to the operating frequency, and then applied to the PA input. Fig. 2.4 represents the simplified block diagram of a predistortion configuration.

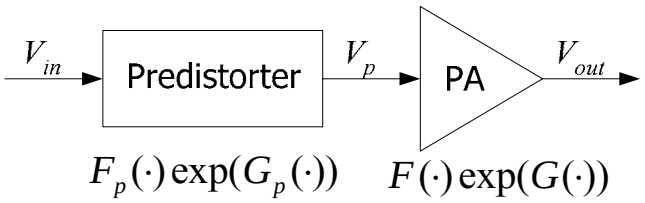


Fig. 2.4. Block diagram of a predistorter

Assuming that the PA is mainly distorted by AM/AM and AM/PM effects, the predistortion function can be found analytically or numerically so that

$$\begin{aligned} V_{out} &= F(V_p)\exp(G(V_p)) \\ &= F(F_p(V_{in}))\exp(G(G_p(V_{in}))) \\ &= gain \cdot V_{in}. \end{aligned} \tag{2.12}$$

Therefore, the amplitude and phase predistortion functions are defined as

$$\begin{aligned} F_p(V_{in}) &= F^{-1}(gain \cdot |V_{in}|), \\ G_p(V_{in}) &= G^{-1}(\angle V_{in}). \end{aligned} \tag{2.13}$$

Practically, the generation of inverse function can be performed accurately by polynomial functions or look-up tables (LUTs), and both methods have advantages and disadvantages in terms of complexity and speed. The most powerful advantage of the polynomial method is simplicity. Even though the order of nonlinearity for a complete inverse function reaches infinity in principle, the truncated polynomial predistorters with about 10-20 parameters have shown reasonable accuracy [10]. Alternatively, LUT-based predistorters have the major advantage of minimal-delayed correction of the signal; having stored the corresponding correction in the tables, the input signal can be modified with processing delays of only a few clock cycles. Moreover, arguably the more stable

operation of the LUT methods has made this architecture dominant in commercial application.

In general, the RF PAs used in such systems are operated in class-AB as a means of trading off linearity for efficiency in situations in which strong nonlinearity is occurring. Nevertheless, despite the presence of strong nonlinearities, incorporating these techniques into the system has the potential to suppress intermodulation distortion (IMD) products by 10-20 dB [50], [51]. Besides PAs, some researchers have also examined the characterization and predistortion of frequency mixers [52]-[55]. One noticeable work was done by Kumar *et al.,* who adopted digital-based predistortion for direct modulation of a phase-shift keying (PSK) signal [56]. As for frequency multipliers, on the other hand, little attention has been paid to applying predistortion techniques to linearize them. Most of the research has focused on their optimal design for better conversion loss during saturated-region operation.

2.3.3 Crest Factor Reduction Technique

One noticeable fact about predistortion is that the technique is most powerful where soft compression begins, and thus performance degrades as the magnitude of the input signal increases. Consequently, carefully modifying the characteristic of the input signal so that the signal is statistically favorable to PAs, a process called crest factor reduction (CFR), is gaining considerable attention in the latest digital signal transmissions [57], [58].

Crest factor (CF) and peak-to-average power ratio (PAPR) are measures to indicate statistically the level of stress a modulated signal imposes on an amplifier that is operating near its maximum output power. These two metrics are defined below.

$$CrestFactor = \frac{\max\{|v(t)|\}}{\sqrt{mean\{|v(t)|^2\}}} \tag{2.14}$$

$$PAPR = \frac{\max\{|v(t)|^2\}}{mean\{|v(t)|^2\}} \tag{2.15}$$

Table 3 represents some examples of PAPR values of different modulation standards [6].

Table 3. Peak-to-average ratios of different modulation schemes.

Modulation Scheme	Parameter	PAPR [dB]
WCDMA1	16 channels	10.5
	64 channels	12.2
	128 channels	13.6
π/4 DQPSK2	α = 0.25	4.55
	α = 0.35	3.87
	α = 0.50	3.21
16-QAM3	α = 0.25	5.92
	α = 0.35	5.40
	α = 0.50	4.94
GSM EDGE (8 PSK)4	–	3.21

Note:
1. Chip rate of 4.096Mcps, RRC filter of α=0.22, statistically independent pseudo-random data.
2. Symbol rate of 24.3ksps, RRC filter, DAMPS coding.
3. Symbol rate of 25ksps, RRC filter, no coding.
4. ETSI SMG2 technical doc. WPB 386/98.

Notice that the higher PAPR or CF is, the higher the maximum power of a signal is. That is, for an amplifier to transmit a signal without distortion, it should be able to handle peak power with zero or minimum compression. However, in reality, the capability to handle infrequent peak signals means extra cost for expensive PAs. Moreover, since recent digital-communication standards tend to be spectrally efficient to accommodate more users or data within the limited frequency resource, these standards like WCDMA or OFDM signals have high PAPR of up to 13 dB. As a result, the PAs that are used must have either a high peak power rating in order to maintain linearity or their output must be reduced, a step that leads to less efficiency and higher operating cost. However, lowered peak-to-average-power-ratios permit the use of PAs with lower power ratings, which means significant cost reduction in a transmitter, especially for a high-power amplifier. Hence, there has been intensive investigation into PAPR reduction and CFR techniques such as code selection, digital clipping or mapping, and pulse injection [6].

To verify if the CFR technique in addition to the predistortion technique can further improve linearity, the CFR and LUT-based digital predistortion techniques were applied to a 30W PA module from CREE Microwave. The PA operates at 1.96 GHz, and the PAPR of the IS-95B input signal is 9.6 dB when no CFR is applied, and it is reduced to 5 dB after the CFR process. Fig. 2.5 shows the measured adjacent-channel power-ratio (ACPR) results for four cases of operation: with and without predistortion with the CFR process, and with and without predistortion without the CFR process.

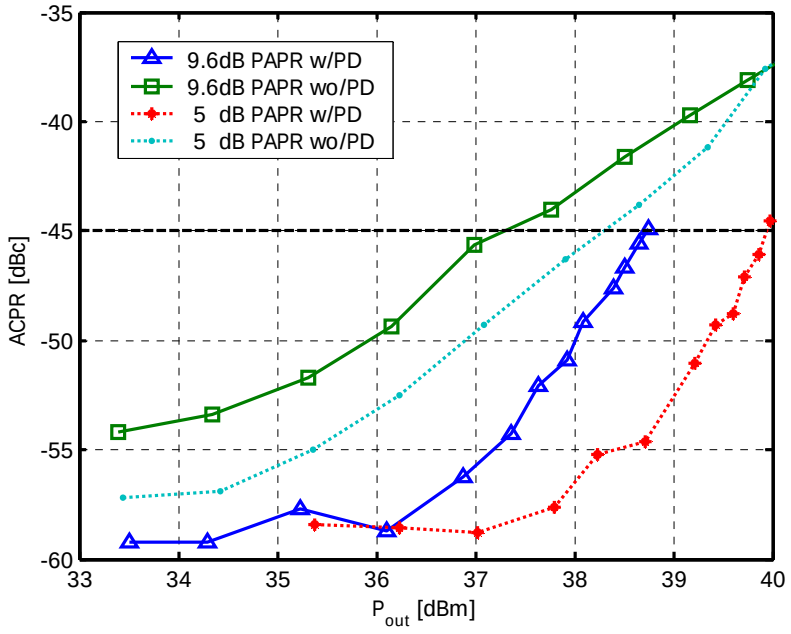


Fig. 2.5. ACPR improvement with respect to output power.

From this figure, we can see that the increase in the output power for the 45 dBc ACPR specification in the IS-95B standard is 1.5 dB with predistortion, and an additional 1.3 dB increase can be achieved by the CFR processed data. This improvement in the output power also means an efficiency improvement, which is directly related to the operational cost of a base station. The lower limit of ACPR in this figure is because of the dynamic range limitation of the test-bed; otherwise, the ACPR results would have been even better than shown. Table 4 shows the efficiency improvement for the four cases of Fig. 2.5. The overall drain efficiency shows an improvement of 5.6% when both CFR and predistortion is applied.

Table 4. Power and efficiency improvement with CFR and predistortion.

	With PD		Without PD	
PAPR	9.6 dB	5 dB	9.6 dB	5 dB
Pout	38.7 dBm	40.0 dBm	37.3 dBm	38.3 dBm
Efficiency	21.5%	23.9%	18.3%	20.5%

2.4 CONCLUSIONS

The theoretical background of frequency multipliers has been discussed in this section, along with their application to frequency converting devices. When high frequency signal sources are required, the direct generation of the signal with crystal oscillators generally is not an optimal solution because of the degraded Q-factor and relatively poor frequency accuracy [9]. In that case, placing a frequency multiplier after a simple crystal oscillator might be a better choice in terms of phase noise and stability, even though the multiplication process degrades the phase noise proportionally to the square of the multiplication number. Even better, the noise figure of the amplifying transistor can be kept low if the oscillator is operated at a sub-multiple of the required output frequency.

Resistive frequency multipliers are inherently broadband but introduce high loss compared to SRDs or reactive type multipliers, whose theoretical efficiency can reach 100%. A huge amount of recent research has been directed at active frequency multipliers, largely because of their positive gain and compatibility with semiconductor technologies.

Nonlinearity in a device is the source of harmonic generation of the carrier frequency, intermodulation distortion of the modulated signal, and other intermodulation distortion that can occur among all of these. In particular, in the case of memoryless nonlinear devices, the amplitude and phase of the signal generate compound modulations classified as AM/AM, AM/PM, PM/AM, and PM/PM. Of these, PM/AM has the least effect and can be neglected in most analyses of nonlinear devices.

Because of recent improvements in DSP performance, digital predistortion is one of the most promising techniques for overcoming undesired distortion from nonlinearity. This technique intentionally applies distortion to the baseband-modulated signal to minimize the distortion after PAs or frequency multipliers.

CFR can be a supplementary technique used in conjunction with predistortion to further reduce distortion caused mainly by the gain compression of devices such as PAs. By manipulating the way a digital code is generated or by suppressing instances of peak power, this technique reduces the signal's overall PAPR, which tends to be large for most advanced communication standards. This reduction allows a PA to amplify a signal with relatively low compression; otherwise, the compressed region in a PA would generate a lot of AM/AM and AM/PM distortion at high-powered peaks of the signal. However, measures must also be taken to minimize the increase in the noise figure that occurs with the CFR process.

CHAPTER 3

ADAPTIVE DIGITAL PREDISTORTION OF FREQUENCY MULTIPLIERS

3.1 INTRODUCTION

Relatively little attention has been given to using frequency multipliers as frequency translation devices for digitally modulated signals when most of the research into frequency multipliers has focused on achieving optimal design to minimize conversion loss during their saturated operation. .

This chapter will present the first results from applying adaptive digital predistortion to frequency multipliers for the transmission of complex modulated signals. Two frequency multipliers of different orders were tested to validate our theory. A derivation of bandpass frequency multiplication was developed and is presented in Section 3.2, and a description of the adaptive predistortion algorithms used for the identification and predistortion of frequency multipliers is also given in Section 3.3. Section 3.4 and

Section 3.5 show the simulation and measurement results of the predistorted frequency multipliers.

3.2 ZONAL TRANSFER CHARACTERISTICS OF FREQUENCY MULTIPLIERS

A complex-modulated bandpass input signal can be represented as

$$\begin{aligned} x(t) &= \mathrm{Re}\left[x_L(t)\cdot e^{j\omega_o t}\right] \\ &= A(t)\cos(w_o t + \theta(t)), \end{aligned} \tag{3.1}$$

where $x_L(t)$ is the complex baseband signal with magnitude $A(t)$ and phase $\theta(t)$. When this signal is fed into a memoryless nonlinear device, its output can be expressed by the power series

$$\begin{aligned} y(t) &= \mathrm{Re}\left\{\sum_{n=0}^{\infty} a_n \left[x_L(t)\cdot e^{j\omega_o t}\right]^n\right\} \\ &= \mathrm{Re}\left\{\sum_{n=0}^{\infty} a_n \left[A(t)\cdot e^{j\omega_o t+\theta(t)}\right]^n\right\}, \end{aligned} \tag{3.2}$$

where a_n is a complex power series coefficient.

Note that this is the baseband representation including all the harmonics generated from the device's nonlinearity. In most cases, we are interested only in one bandpass zone: the fundamental frequency for PAs and the n^{th} zone for frequency multipliers. The relationship between the input and output at the fundamental frequency (first-zone response) has been obtained [59]. For the extraction of the n^{th} zone response, only odd harmonic responses will be taken into account. Applying the Chebyshev Transform [60]

to (3.2), the n^{th} zone response can be described as below, and distortions can be identified by truncated power series forms of the highest-order Q.

$$\begin{aligned}\tilde{y}_n(t) &\cong \mathrm{Re}\left[\sum_{m=(n-1)/2}^{(Q-1)/2} \frac{a_{2m+1}}{2^{2m}} \binom{2m+1}{m+\frac{n+1}{2}} \left|x_L(t)\right|^{2m-n+1} x_L^n(t)\, e^{jnw_o t}\right] \\ &= \mathrm{Re}\left[\sum_{m=(n-1)/2}^{(Q-1)/2} \frac{a_{2m+1}}{2^{2m}} \binom{2m+1}{m+\frac{n+1}{2}} A(t)^{2m+1} e^{jn\theta(t)}\, e^{jnw_o t}\right], \\ &= \mathrm{Re}\left[g(A(t)) e^{j(nw_o t + n\theta(t) + f(A(t)))}\right]\end{aligned} \tag{3.3}$$

where

$$\begin{aligned} g(A(t)) &= \left|\sum_{m=(n-1)/2}^{(Q-1)/2} \frac{a_{2m+1}}{2^{2m}} \binom{2m+1}{m+\frac{n+1}{2}} A(t)^{2m+1}\right|, \\ &= \sum_{m=(n-1)/2}^{(Q-1)/2} a'_{2m+1} A(t)^{2m+1} \end{aligned} \tag{3.4}$$

$$\begin{aligned} f(A(t)) &= \arctan\left\{\frac{\mathrm{Im}\left[\sum_{m=(n-1)/2}^{(Q-1)/2} \frac{a_{2m+1}}{2^{2m}} \binom{2m+1}{m+\frac{n+1}{2}} A(t)^{2m+1}\right]}{\mathrm{Re}\left[\sum_{m=(n-1)/2}^{(Q-1)/2} \frac{a_{2m+1}}{2^{2m}} \binom{2m+1}{m+\frac{n+1}{2}} A(t)^{2m+1}\right]}\right\} \\ &= \sum_{m=(n-1)/2}^{(Q-1)/2} b'_{2m+1} A(t)^{2m+1}. \end{aligned} \tag{3.5}$$

Equations (3.4) and (3.5) represent AM/AM and AM/PM distortions, and they are approximated by a truncated power series with real coefficients a'_{2m+1} and b'_{2m+1}, respectively. It is noticeable that in the AM/AM distortion function $g(\cdot)$, generally the dominant term is related to $A(t)^n$, resulting in the power transfer slope of n:1 in the dB scale.

In addition to the conventional distortion from the device's nonlinearity, another distortion, which we call PM/PM distortion, arises from the frequency multiplication process. This can be seen in (3.3), where $\theta(t)$ is multiplied by n. From the above equations, we can get the fundamental-zone transfer function, which represents the nonlinearity in amplifiers, and the second- and the third-zone transfer functions, which are useful in the analysis of nonlinearity from frequency multipliers. These transfer functions are shown below.

$$y(t) = \mathrm{Re}\left[\sum_{m=0}^{\infty} \frac{a_{2m+1}}{2^{2m}} \binom{2m+1}{m+1} \left|x_L(t)\right|^{2m} x_L(t)\, e^{j2\pi f_o t}\right] : \text{Fundamental Zone} \quad (3.6)$$

$$y(t) = \mathrm{Re}\left[\sum_{m=1}^{\infty} \frac{a_{2m}}{2^{2m-1}} \binom{2m}{m+1} \left|x_L(t)\right|^{2m-2} x_L^2(t)\, e^{j2\pi 2 f_o t}\right] : \text{Second Zone} \quad (3.7)$$

$$y(t) = \mathrm{Re}\left[\sum_{m=1}^{\infty} \frac{a_{2m+1}}{2^{2m}} \binom{2m+1}{m+2} \left|x_L(t)\right|^{2m-2} x_L^3(t)\, e^{j2\pi 3 f_o t}\right] : \text{Third Zone} \quad (3.8)$$

In frequency multipliers, noise analysis can be done more conveniently by adopting the modulation transfer matrix [61].

$$\begin{bmatrix} m_{out} \\ \theta_{out} \end{bmatrix} = \begin{bmatrix} T_{aa} & T_{ap} \\ T_{pa} & T_{pp} \end{bmatrix} \begin{bmatrix} m_{in} \\ \theta_{in} \end{bmatrix} + \begin{bmatrix} m_{add} \\ \theta_{add} \end{bmatrix}, \quad (3.9)$$

where m and $\theta(t)$, respectively, are the amplitude and phase modulations. The subscripts *in* and *out* mean input and output; the subscript *add* means the noise is an additive component. The basic assumptions are that the noise is stationary and Gaussian, which is assumed to be effective for our cases. The Ts represent AM/AM, PM/AM, AM/PM, and PM/PM modulation transfer coefficients. By expanding this modulation

transfer matrix to handle nonlinear distortions as described above, and by limiting the highest order of nonlinear series to Q, (3.3) and (3.9) can be combined as

$$\begin{bmatrix} m_{out}(t) \\ \theta_{out}(t) \end{bmatrix} = \begin{bmatrix} \mathbf{G} & 0 \\ \mathbf{F} & n \end{bmatrix} \begin{bmatrix} \mathbf{M} \\ \theta_{in}(t) \end{bmatrix}, \tag{3.10}$$

where

$$\begin{aligned} \mathbf{G} &= \begin{bmatrix} a_n' & a_{n+2}' & \dots & \dots & a_Q' \end{bmatrix} \\ \mathbf{F} &= \begin{bmatrix} b_n' & b_{n+2}' & \dots & \dots & b_Q' \end{bmatrix} \\ \mathbf{M} &= \begin{bmatrix} A(t)^n & A(t)^{n+2} & \dots & A(t)^Q \end{bmatrix}^T. \end{aligned} \tag{3.11}$$

$\mathbf{G}$, $\mathbf{F}$ are coefficient matrices to represent $g(\cdot)$ and $f(\cdot)$ as in (3.4) and (3.5); $\mathbf{M}$ is the input-magnitude vector.

Because in frequency multipliers the noise contribution resulting from the noise figure and low frequency phase modulation is negligible compared with the nonlinear distortion components, the additive noise vector was dropped in (3.10). This extended transfer matrix enables us to easily express and understand the distortion that arises from nonlinear frequency multipliers. In applying (3.10), the resulting output n^{th} zone output signal is expressed as

$$\tilde{y}_n(t) = \mathrm{Re}\left[m_{out}(t) e^{j\theta_{out}(t)} e^{j\omega_c t} \right]. \tag{3.12}$$

The next section discusses the methods used to derive the original input signal from the output described in (3.12).

3.3 ADAPTIVE PREDISTORTION METHODS

3.3.1 Modulation Transfer Method

As shown in Fig. 3.1 and based on (3.10), the predistortion system's input and output relations are represented by

$$\begin{aligned} \mathbf{Z}_o &= \mathbf{T}_p \mathbf{X}_i \quad \text{: Predistorter,} \\ \mathbf{Y}_o &= \mathbf{T}_g \mathbf{Z}_i \quad \text{: Nonlinear device,} \end{aligned} \tag{3.13}$$

where

$$\mathbf{T}_p = \begin{bmatrix} \mathbf{G}_p & 0 \\ \mathbf{F}_p & n_p \end{bmatrix}, \text{and } \mathbf{T}_g = \begin{bmatrix} \mathbf{G}_g & 0 \\ \mathbf{F}_g & n_g \end{bmatrix} \tag{3.14}$$

are the modulation transfer-coefficient matrices for the predistorter and nonlinear device, respectively;

$$\begin{aligned} \mathbf{Z}_o &= \begin{bmatrix} m_Z \\ \theta_Z \end{bmatrix}, \ \mathbf{Y}_o = \begin{bmatrix} m_Y \\ \theta_Y \end{bmatrix}, \\ \mathbf{X}_i &= \begin{bmatrix} \mathbf{M}_\mathbf{X} \\ \theta_X \end{bmatrix}, \text{ and } \mathbf{Z}_i = \begin{bmatrix} \mathbf{M}_\mathbf{Z} \\ \theta_Z \end{bmatrix} \end{aligned} \tag{3.15}$$

are the output and input vectors as defined in (3.10).

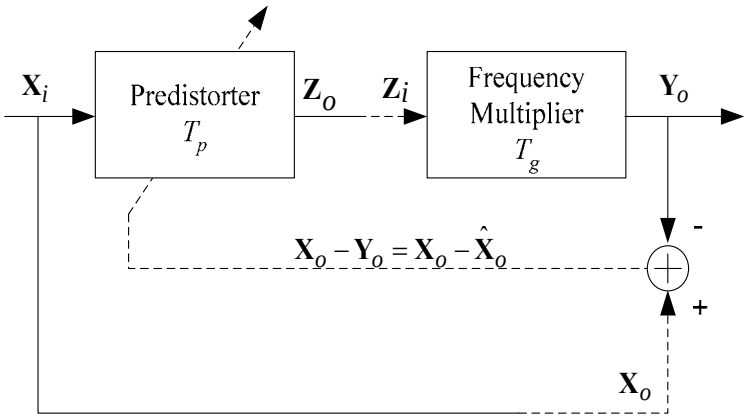


Fig. 3.1. Block diagram of an adaptive predistorter.

The device's modulation transfer matrix $\mathbf{T}_g$ is found by the least-squares method from measured data $\mathbf{Y}_o$ and $\mathbf{Z}_i$ that are measured at the input and output of the device:

$$\mathbf{T}_g = \mathbf{Z}_i \mathbf{Y}_o^T (\mathbf{Y}_o \mathbf{Y}_o^T)^{-1}. \tag{3.16}$$

Moreover, the predistortion transfer matrix $\mathbf{T}_p$ is calculated in the same way,

$$\mathbf{T}_p = \mathbf{Z}_o \mathbf{Y}_i^T (\mathbf{Y}_i \mathbf{Y}_i^T)^{-1}, \tag{3.17}$$

where $\mathbf{T}_p$ represents the inverse of the nonlinear function when $\mathbf{Y}_i$ is the measured output of the nonlinear device formed as the input vector in (3.15). However, since the statistical distribution of $\mathbf{Y}_i$ is not the same as $\mathbf{X}_i$ that is the input of the predistorter, the $\mathbf{T}_p$ matrix calculated by (3.17) does not provide the best pre-inverse function for the predistortion system. Therefore, an iterative method may be employed to improve $\mathbf{T}_p$

to find the solution that minimizes the cost function and provides a better solution for the given measured input and output data.

Among many available iterative methods, the least mean square (LMS) method is one of the most popular algorithms. The *k*th transfer matrix $\mathbf{T}_{p,k}$ is calculated by

$$\mathbf{T}_{p,k+1} = \mathbf{T}_{p,k} + \mu \cdot \frac{\partial \xi_k(\mathbf{T}_{p,k})}{\partial \mathbf{T}_{p,k}}, \tag{3.18}$$

where

$$\xi_k(\mathbf{T}_{p,k}) = \left(\mathbf{X}_{o,k} - \mathbf{Y}_{o,k}\right)^2 \tag{3.19}$$

is the *k*th cost function to be minimized by iteration, and $\mathbf{X}_{o,k}$, $\mathbf{Y}_{o,k}$ are *k*th output matrices.

Another way to find the inverse of a nonlinear device is by iterative-generation of a look-up table (LUT) based on measured input and output data. Although it may introduce errors from the quantization of LUT indices, it can theoretically find an inverse solution for any order of nonlinearity. Moreover, the LUT-quantization error can be reduced by compromising the convergence time and the number of input indices [50].

3.3.2 Simulation of LUT-based Predistortion

To show the improvements of an adaptive predistortion system, the Schottky-diode frequency tripler was simulated with an adaptive LUT-based predistorter implemented in Agilent ADS. The model included separate LUTs for amplitude and phase corrections. However, the operation of the phase LUT differs from the conventional AM/PM LUT

because the PM/PM distortion exists as well as the usual AM/PM distortion. Fig. 3.2 shows the functional block diagram of the predistorter.

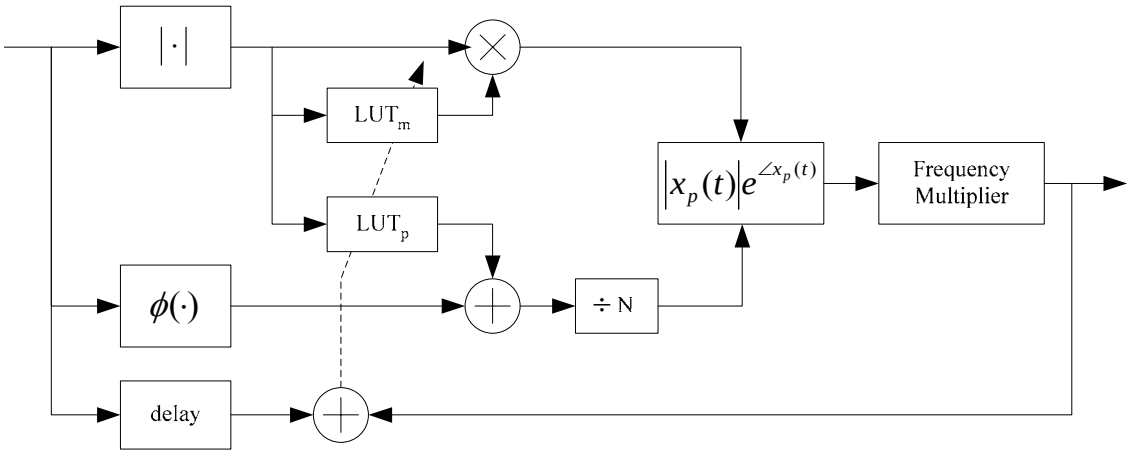


Fig. 3.2. Block diagram of LUT-based predistorter of a frequency multiplier.

A four-tone test signal was used for the simulation. The tones were separated by 1.07 MHz on each side, with a 2.14 MHz separation in the middle. The PAPR of the signal was 6.1 dB, about the same as the CDMA signal that will be discussed in the next section. Fig. 3.3 shows the results with and without the predistortion. As shown in this figure, the IMD without predistortion dramatically increased the bandwidth of the original input signal. After predistortion, the third-order IMD was improved to better than 40 dBc over a bandwidth of more than three times the input signal bandwidth. Further improvement in IMD was limited by the dynamic range of the original signal.

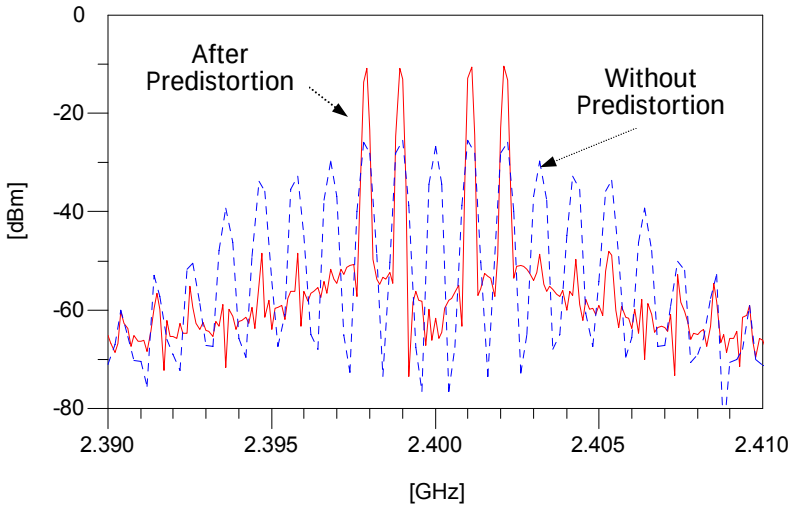


Fig. 3.3. Simulated output spectrum of LUT-based predistorter for a frequency tripler with a four-tone input.

Fig. 3.5 shows the LUT entry after simulation, and this represents the gain versus input magnitude. Because the major predistortion gain should compensate for the third-order distortion, the predistortion gain has to be dominated by the form $\sqrt[3]{1/x^2}$ as shown in Fig. 3.4, and the simulated result in Fig. 3.5 validates this expectation.

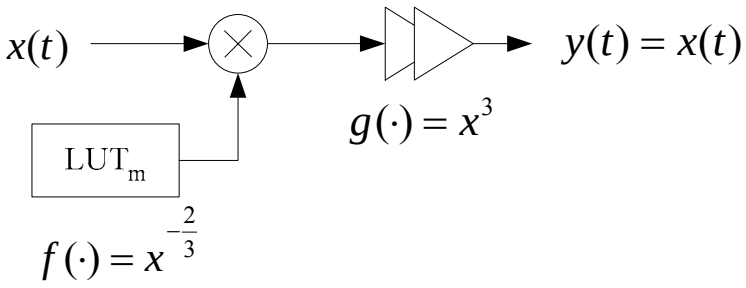


Fig. 3.4. Estimation of look-up table entry for a multiplicative predistorter assuming dominant third-order nonlinearity.

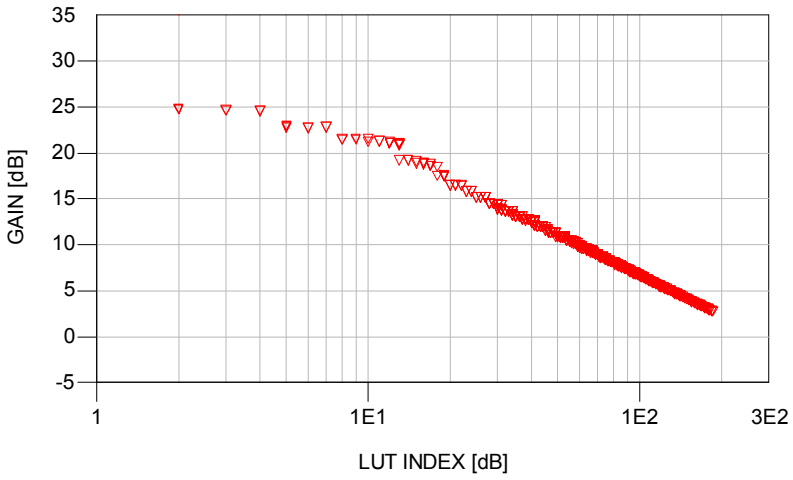


Fig. 3.5. Simulated LUT results for the 4-tone input after adaptive predistortion of the frequency tripler.

3.4 EXPERIMENTAL VALIDATION

For the validation of our predistortion theory, two different devices were examined. A Schottky-diode frequency tripler was designed by the author for an output of 2.46GHz, as shown in Fig. 3.6. The Schottky-diodes are Agilent's HSMS-2852. In addition, a Mini-Circuits MK-2 frequency doubler was purchased and tested to produce an output at 820MHz. The assembled tripler is shown in Fig. 3.7.

For characterization of the device, a continuous wave input signal at 820 MHz was fed into the frequency tripler and power swept to measure its fundamental zone and third-zone output power. The results are shown in Fig. 3.8. As expected, the third-zone curve shows a 3:1 slope over a range of almost 15 dB. Beyond this range, the slope is compressed because of the saturation of current through the Schottky-diodes, producing

relatively strong higher-order harmonics. In contrast, a slope of almost 4:1 was observed with the Mini-Circuits doubler on the second-zone responses, as shown in Fig. 3.9, indicating strong nonlinearity was occurring.

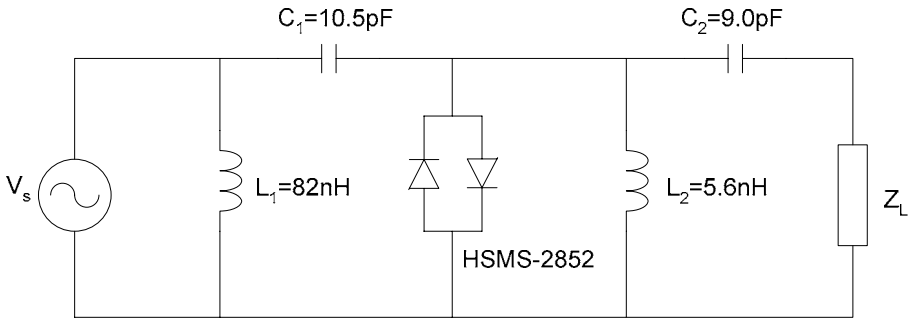


Fig. 3.6. Schematic of the Schottky-diode frequency tripler.

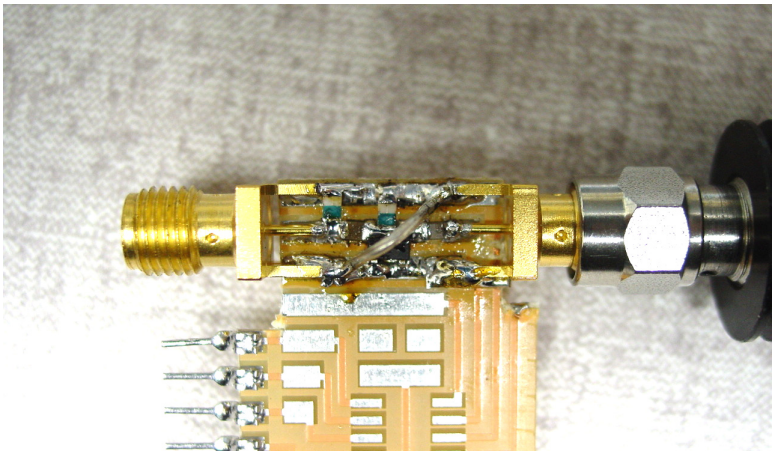


Fig. 3.7. Picture of assembled Schottky-diode frequency tripler.

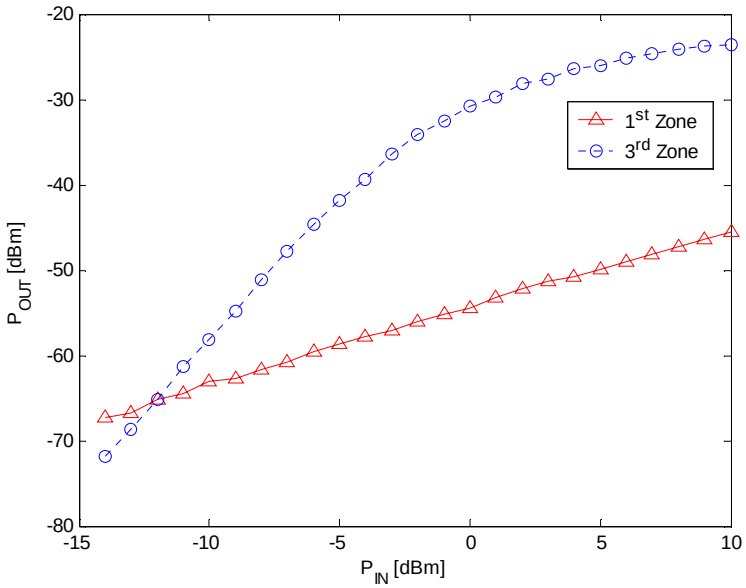


Fig. 3.8. First- and third-zone transfer characteristics of the diode tripler.

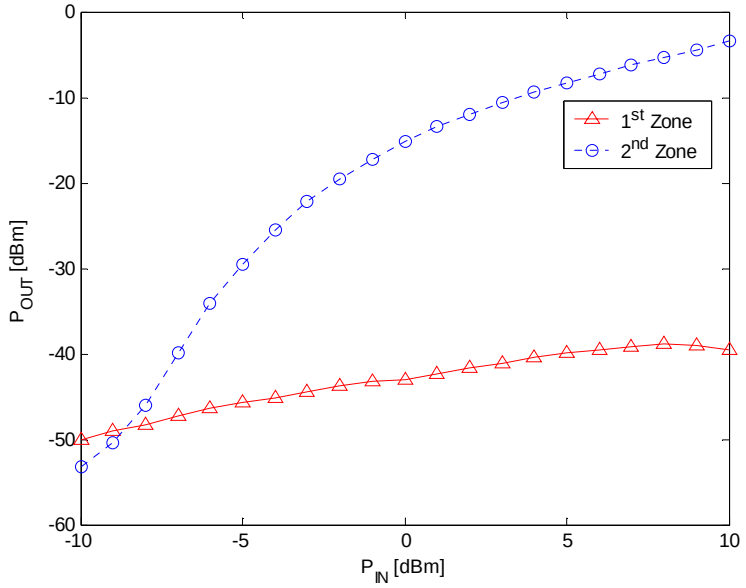
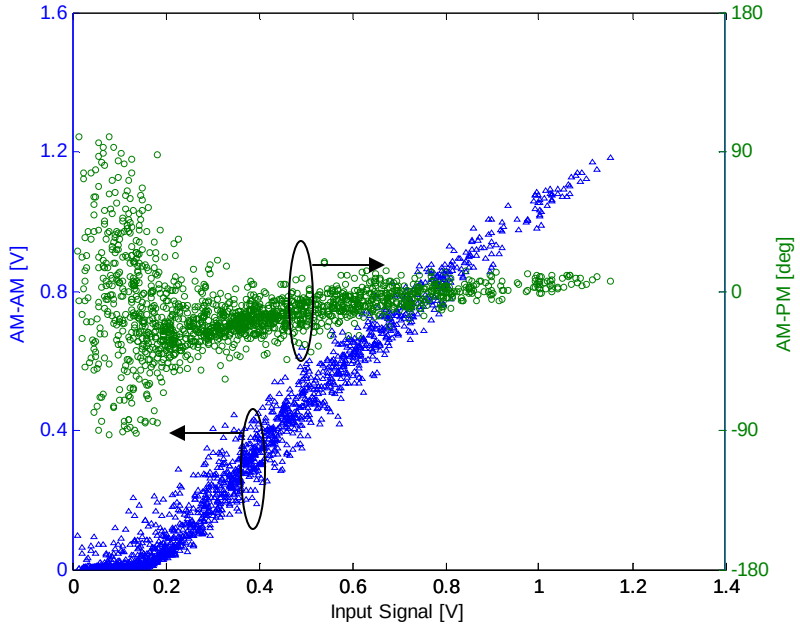


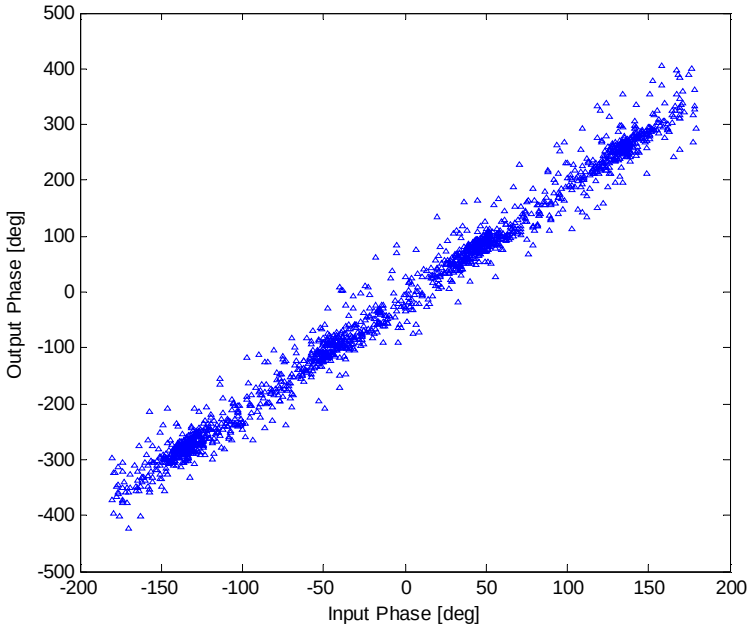
Fig. 3.9. First- and second-zone transfer characteristics of the diode doubler.

For the extraction of AM/AM, AM/PM, and PM/PM responses, a quadrature-modulated signal was fed into the devices, and the output signal was downconverted to an IF frequency. Then it was digitized and demodulated. By comparing magnitudes and phases of input and output signals, AM/AM, AM/PM, and PM/PM responses can be calculated to form (3.10).

The extracted responses for each device are illustrated in Fig. 3.10 and Fig. 3.11. From this data, we can clearly see that the amplitude and phase nonlinearities are much more severe than those in PAs. Also, note in the PM/PM graph that the slope of the asymptotic line represents the phase multiplication. The bunching of data points occurs because the input is an oversampled quadrature phase shift keying (QPSK) signal. For lower input levels, the output amplitude is nearly zero because of the turn-on voltage of the Schottky diodes. As a result, phase measurements have relatively high variances at lower inputs. Although passive diode multipliers serve as useful circuits to validate the theory, the conversion loss is quite high in the range of dominant third- or second-order operation. A more practical approach might be to use active elements (BJTs or MESFETs) to achieve some conversion gain in the harmonic generation processes.

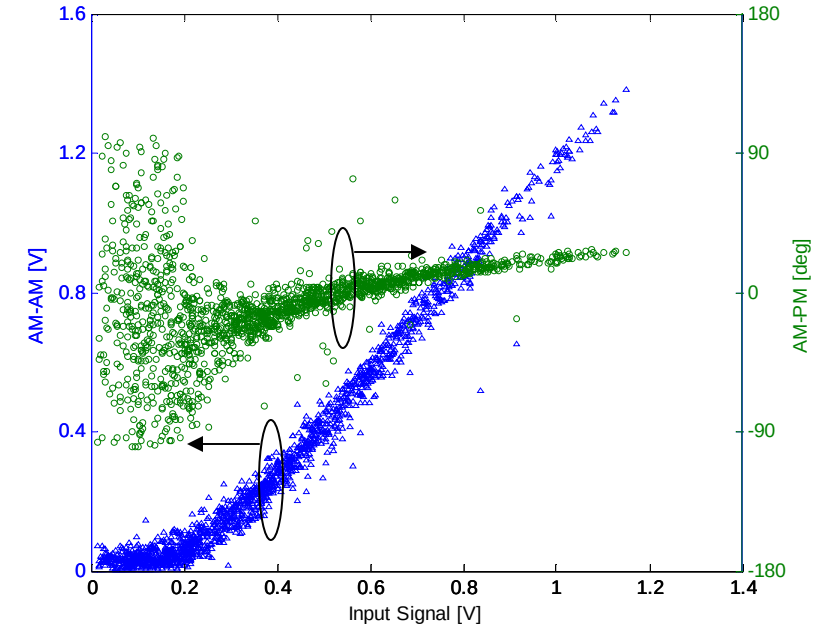


(a)

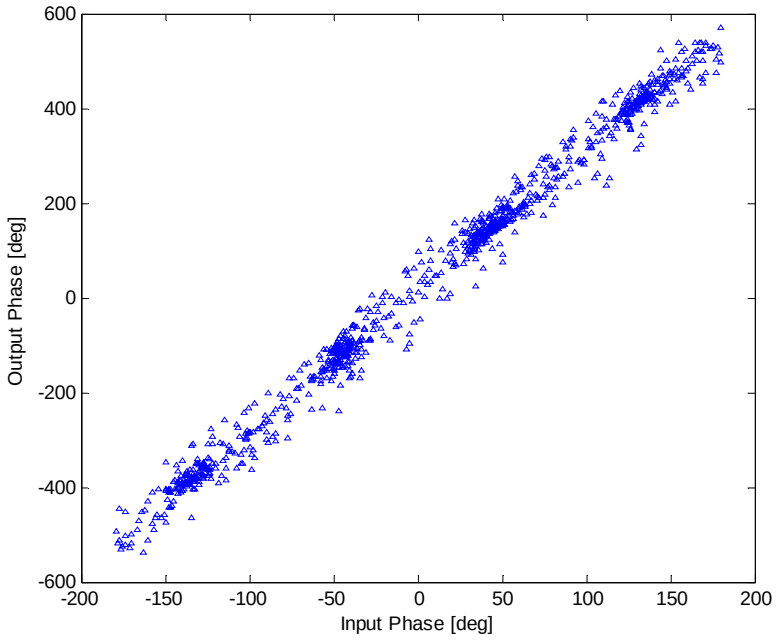


(b)

Fig. 3.10. Characteristics of the frequency doubler. (a) AM/AM, AM/PM responses. (b) PM/PM response.



(a)



(b)

Fig. 3.11. Characteristics of the frequency tripler. (a) AM/AM, AM/PM responses. (b) PM/PM response.

For the predistortion of the previously mentioned frequency multipliers, a polynomial-based adaptive digital predistorter was built to find the exact memoryless-nonlinear models of the devices and then to predistort them. As described in the previous section and represented in Fig. 3.12, a complex modulated signal is generated in a PC and then loaded into an Agilent E4432B arbitrary waveform signal generator. For each of the frequency multipliers, the predistortion modulation transfer matrix $\mathbf{T}_p$ was extracted from the measured data. Based on $\mathbf{T}_p$, a predistorted signal set was generated, loaded into E4432B, and upconverted to RF. The original input was an IS-95B forward channel signal at 820 MHz for the tripler and 410 MHz for the doubler. The output signals were taken at 2.46 GHz, and 820 MHz, respectively. To further guarantee the convergence of the polynomial-based predistorter, a LUT-based predistorter was built as well. The LUTs are updated by the LMS method [62]. By comparing the results of the two predistorters, we can see that our theory is applicable to both types of predistorters and be assured that the polynomial can express stably the nonlinearities coming from the frequency multiplication process.

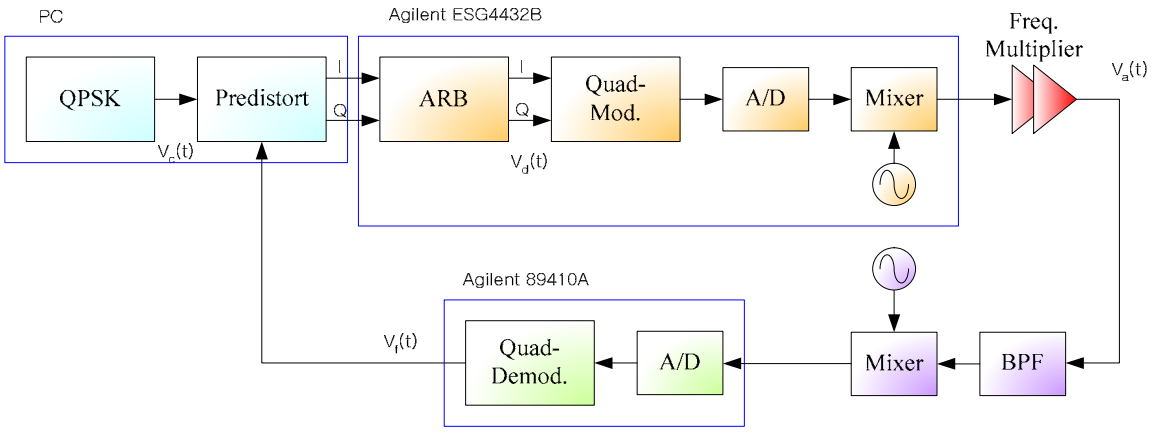


Fig. 3.12. Setup for the adaptive predistortion of frequency multipliers.

The performance of the predistorter was verified by the output spectrums presented in Fig. 3.13 through Fig. 3.15: the predistortion of the tripler is shown in Fig. 3.13. The original uncompensated output signal was widely spread over 3 MHz because of the phase multiplication, resulting in an ACPR of 20 dBc. The adaptive digital predistortion improved the ACPR to 50 dBc at 885 kHz offset from the center frequency. After predistortion, some residual third-order regrowth still exists owing to the truncation in the series. A similar result was observed with the predistortion of the doubler, which is shown in Fig. 3.14.

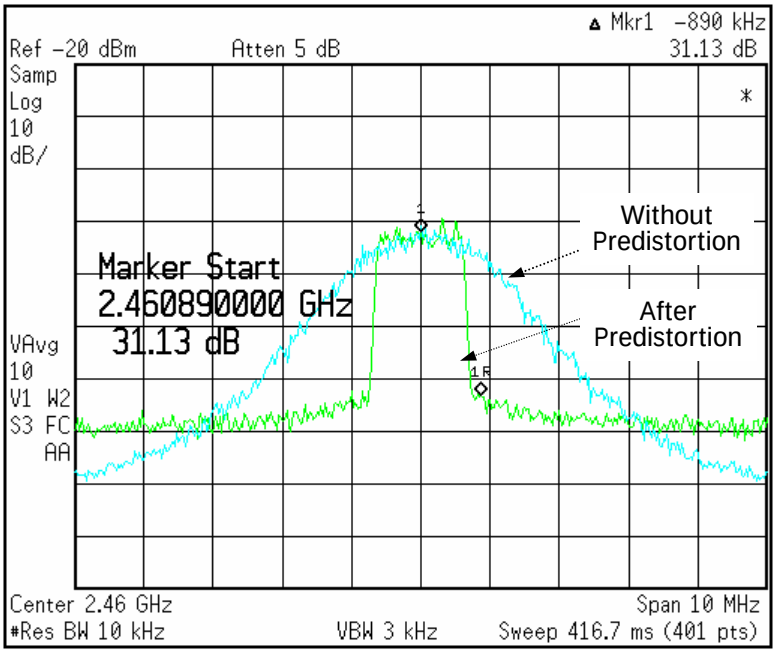


Fig. 3.13. Polynomial-based predistortion result of the frequency tripler.

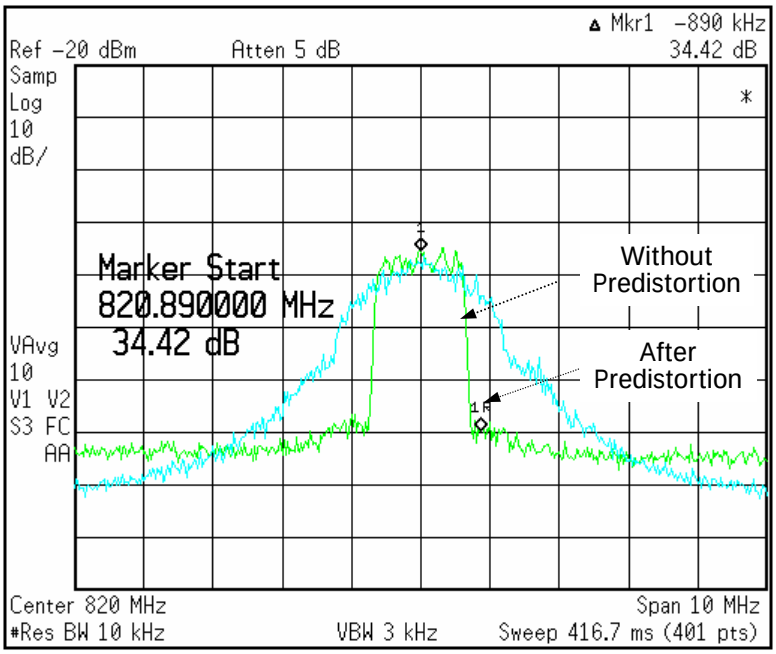


Fig. 3.14. Polynomial-based predistortion result of the frequency doubler.

The result of the LUT-based predistorter of the frequency tripler is in Fig. 3.15, which shows a 3dB better suppression of IMDs. The AM/AM LUT entry after predistortion of the frequency tripler is expressed by dB scales in Fig. 3.16. Notice that the slope is -2/3:1 over 10 dB of the input scale. This verifies the observation in Fig. 3.8 that the dominant slope is 3:1; therefore, as in its multiplicative compensating function, it should have -2/3:1 slope representing a cube root function. The in-band error-vector magnitude (EVM) was reduced from nearly 100% before predistortion to 7.3%, which can be verified from the constellation measurements in Fig. 3.17.

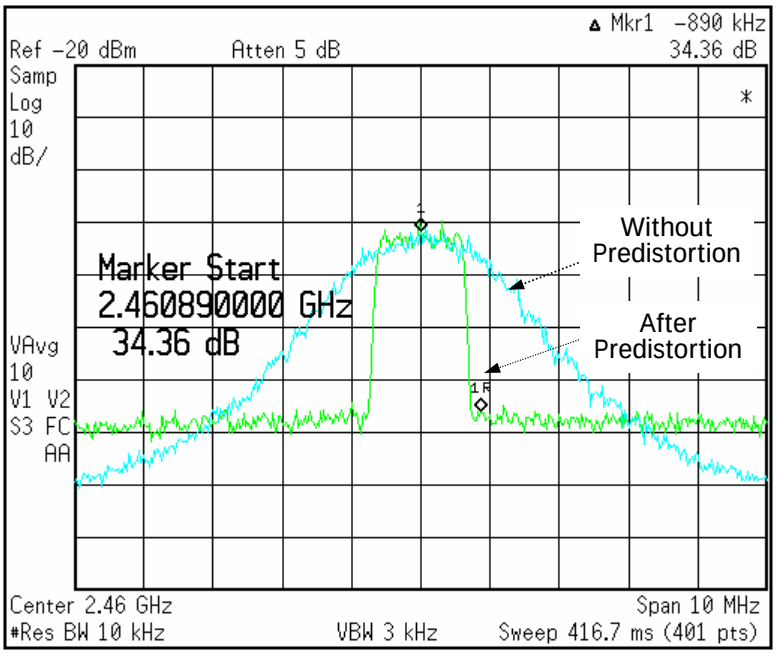


Fig. 3.15. LUT-based predistortion result of the frequency tripler.

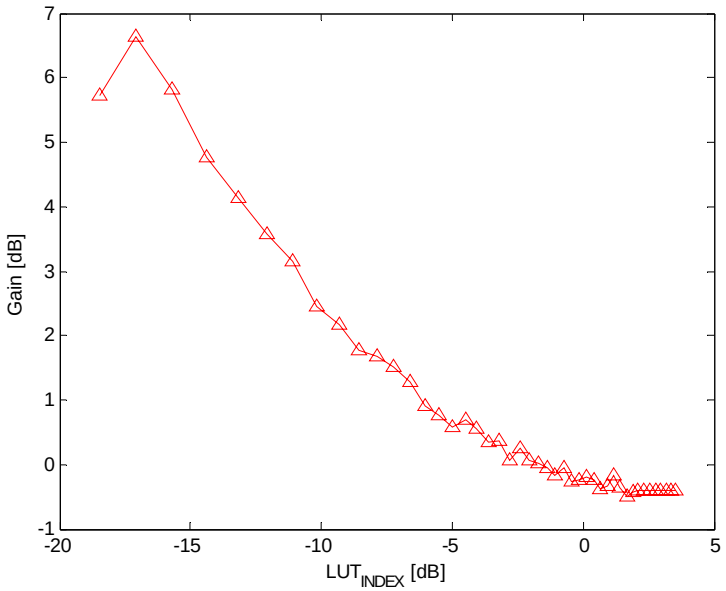
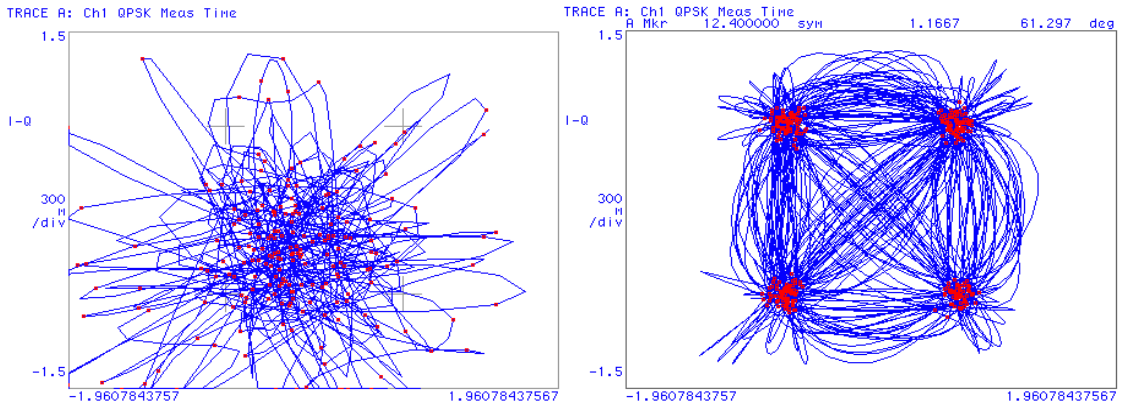


Fig. 3.16. LUT results for an IS-95B input after adaptive predistortion of the frequency tripler.



(a) (b)

Fig. 3.17. Constellation measurements of IS-95B signal (a) Without predistortion (b) After predistortion.

3.5 CONCLUSIONS

This chapter has presented a theory and a demonstration of predistortion linearization applied to frequency multipliers. The theory was based on baseband predistortion of the input envelope, and the estimated response using the extended transfer matrix was introduced to describe distortions related to frequency multipliers. A simulation model of frequency tripler implemented in ADS showed that a LUT-based digital predistorter can adaptively correct for AM/AM, PM/PM, and AM/PM distortion to improve IMD to better than 40 dBc. To verify this theory, a Schottky-diode frequency tripler and doubler at different frequencies were measured for the frequency multiplication of an IS-95B CDMA signal. The frequency tripler showed a 3:1 input and output power relationship for most of the input range, whereas the doubler showed a higher than 2:1 slope, indicating higher order distortions are affecting the second-zone power transfer

characteristics. Moreover, phase multiplications of the baseband signal were observed for both devices. Adaptive digital predistorters, based on polynomial series and LUT algorithms, were implemented to correct the AM/AM, AM/PM, and PM/PM distortions for the second and third zone nonlinearities. The results of the two algorithms, implemented on a test-bed, achieved more than 31 dB improvement of the ACPR with an EVM of 7~8% for all multipliers. Without predistortion, those metrics were approximately 20 dBc and 100%, respectively. The resulting LUT entry from the predistortion of the tripler mainly represents a -2/3:1 slope in logarithmic scale to compensate for the 3:1 slope without any predistortion applied to the device. From the results of our research, we can conclude that it is feasible to use predistorted frequency multipliers to transmit digitally modulated signals.

CHAPTER 4

DUAL-MODE DUAL-BAND TRANSMITTERS

4.1 INTRODUCTION

Any kind of transistor has numerous sources of harmonics such as nonlinear transconductance, gate-source capacitance, and gate-drain capacitance, all of which depend on the input power and on external biasing [63]-[65]. These sources of nonlinearities, all of which are considered detrimental in linear amplification, may be intentionally enhanced or suppressed according to the mode of operation. The best possible solution to handle the nonlinearities in both ways (adversely or intentionally) on a device is to place the transistors in a balanced configuration and control the combination of output currents in combination with proper biasing for each mode. Section 4.2 presents a detailed explanation of this balanced nonlinear device and of the way the input phasing can be used to suppress or emphasize harmonic currents. In Section 4.3, another architecture is discussed that uses a passive low-loss varactor doubler after a PA for second harmonic generation. The doubler can be bypassed using an RF switch to transmit a signal in the fundamental frequency. Although placing a

bypass switch at the output of a PA is not the best choice in terms of additional loss, the overall performance may be acceptable because the conversion loss of the varactor doubler can be kept extremely low, theoretically reaching 100% efficiency [66]-[69], and thus the overall performance may be acceptable. Section 4.4 presents the measurement results. Finally, we compare both approaches and draw conclusions about their advantages in dual-mode handset transmitters.

4.2 ACTIVE DUAL-MODE FREQUENCY DOUBLER

4.2.1 Harmonic Generation

Harmonic generation may be achieved from nonlinear semiconductor devices such as Schottky-barrier diodes, varactor diodes, step-recovery diodes (SRDs), and transistors [20]-[24]. Varactor diodes and SRDs use nonlinear capacitance, so in theory, they can generate harmonic signals without any loss; however, practical use has shown that some degree of loss must be tolerated to achieve reasonable levels of operating bandwidth.

For active MESFET frequency multipliers, controlling the conduction angle of the signal carrier by the gate input voltage is the main source of harmonic signal generation. The maximum harmonic output current of a frequency multiplier of this kind can be expressed as follows by Fourier series expansion [24].

$$I_n(\phi) \approx I_{max} \frac{4\phi}{\pi^2} \cdot \left| \frac{\cos n\phi}{1-(2n\phi/\pi)^2} \right|, \qquad n \geq 1 \tag{4.1}$$

where I_{max} is the maximum input current, n is the harmonic order, and ϕ is half the conduction angle. This equation represents the maximum possible output current that can generate harmonic power at a given conduction angle. Fig. 4.1 represents the resulting normalized harmonic output currents as a function of the conduction angle. However, this interpretation can be misleading from the viewpoint of conversion efficiency because to get the calculated maximum output power the input power must be increased as the conduction angle is decreased-. This increase in the input power may not be feasible in reality because increased input power can damage the input port of a transistor or the correspondingly increased output power with imperfectly terminated harmonics can burn the system out.

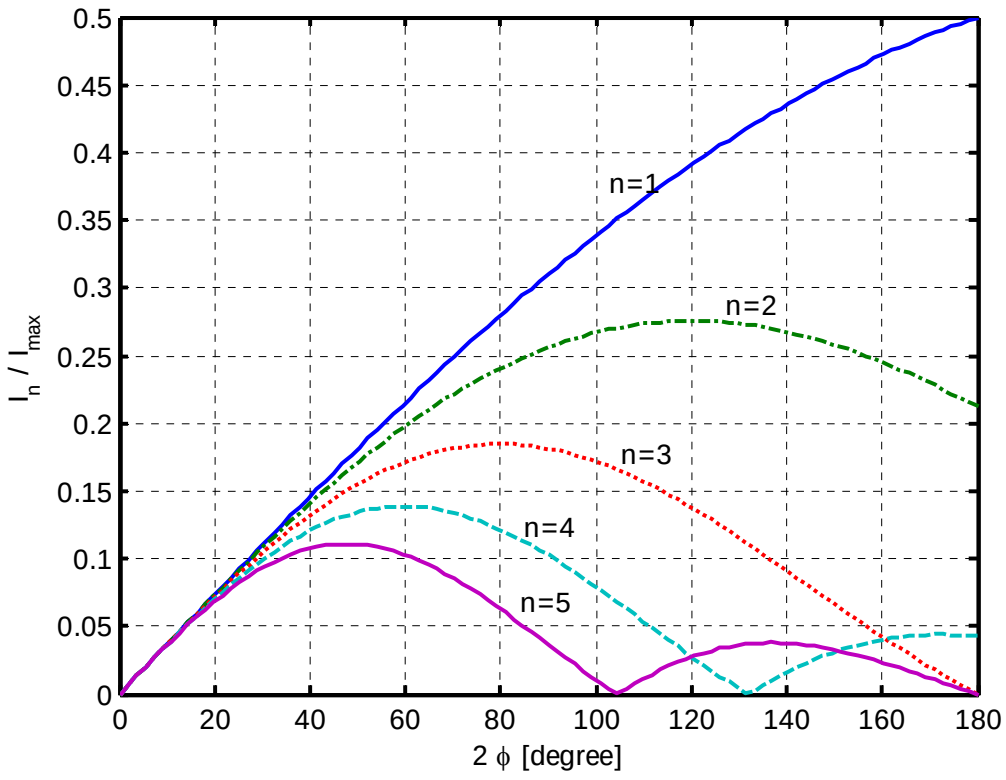


Fig. 4.1. Normalized harmonic output current as a function of conduction angle.

Therefore, to compare the conversion efficiency instead of the maximum output power over the conduction angle, we need to rewrite (4.1) to show the harmonic output currents with the fixed input current.

The output drain current of conduction angle 2ϕ is shown in Fig. 4.2, and can be represented as below.

$$I_d(\theta) = I_{peak}\cos(\theta) - I_{offset}. \tag{4.2}$$

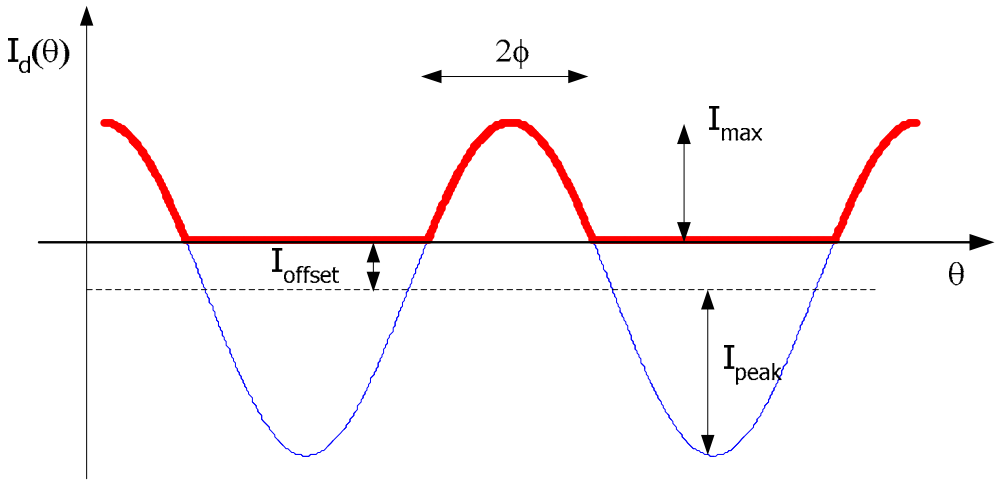


Fig. 4.2. Output current waveform for a single-transistor frequency multiplier.

The conduction angle is defined as

$$\cos(\phi) \equiv \frac{I_{offset}}{I_{peak}}, \tag{4.3}$$

where

$$I_{peak} = I_{max} + I_{offset} . \tag{4.4}$$

Therefore,

$$I_{max} = I_{peak}(1 - \cos(\phi)) . \tag{4.5}$$

Rearranging (4.2) with the above equations, we can get the total drain current composed of two parts: the first part can be expressed by I_{max}, which is the maximum value of output current, or I_{peak}, which represents the amplitude of the sinusoidal swing; the second part $f(\theta,\phi)$ shows the time and conduction angle dependences.

$$\begin{aligned} I_d(\theta,\phi) &= \frac{I_{max}}{1-\cos(\phi)}\left[\cos(\theta) - \cos(\phi)\right] \\ &= \frac{I_{max}}{1-\cos(\phi)} f(\theta,\phi) \end{aligned} \tag{4.6}$$

or

$$\begin{aligned} I_d(\theta,\phi) &= I_{peak}\left[\cos(\theta) - \cos(\phi)\right] \\ &= I_{peak} f(\theta,\phi) \end{aligned} . \tag{4.7}$$

Notice that the Fourier transformed representation of drain current in (4.6) is equivalent to (4.1), whereas (4.7) is different. This is because either I_{max} or I_{peak} in (4.5) is a function of the conduction angle, 2ϕ; expressing I_d by the maximum output current I_{max} leads to (4.6), which means that to keep I_{max} constant the input magnitude I_{peak} should be increased as ϕ decreases. In contrast, when I_d is expressed in terms of conversion loss, the amplitude of the input current I_{peak} is kept constant, and thus from (4.5) I_{max} is decreased when the conduction angle is lowered from 180°, resulting in (4.7). As a

result, the Fourier series expansion of the output current in (4.7) leads to harmonic components, which are expressed as below.

$$I_{d,n}(\phi) = I_{peak} f_n(\phi)$$
$$= \begin{Bmatrix} \frac{I_{peak}}{\pi}\left[\phi - 0.5\sin(2\phi)\right] & : n = 1 \\ \frac{I_{peak}}{\pi}\left\{\left(\frac{1}{n+1} - \frac{1}{n}\right)\sin\left[(n+1)\phi\right] + \left(\frac{1}{n-1} - \frac{1}{n}\right)\sin\left[(n-1)\phi\right]\right\} & : n > 1 \end{Bmatrix}. \quad (4.8)$$

Equation (4.8) represents the situation when the conduction angle is controlled by the gate voltage in a MESFET-based frequency multiplier. Its result is shown in Fig. 4.3, indicating that the minimum conversion loss can be achieved with the conduction angle of 180° for a doubler, 120° for a tripler, and so on. The conversion loss can be calculated from the equation:

$$C.L. = 20\log\left(\frac{Max(I_{d,n}(\phi))}{I_{peak}}\right). \quad (4.9)$$

From the results induced so far, a frequency doubler might be a good choice for a dual-band transmitter because of its relatively low conversion loss. If a frequency doubler is to be so used, methods of implementing reconfigurability between the frequency doubler and the fundamental-mode amplifier by using phase control at the input and output ports of transistors — as shown in Fig. 4.4 — need to be identified, and the results are listed in Table 5. Referring to these table and figure, it can be concluded that providing an overall phase difference of 180° between two signal paths can turn an amplifier into a frequency doubler. However, zero overall phase difference makes the system a regular amplifier.

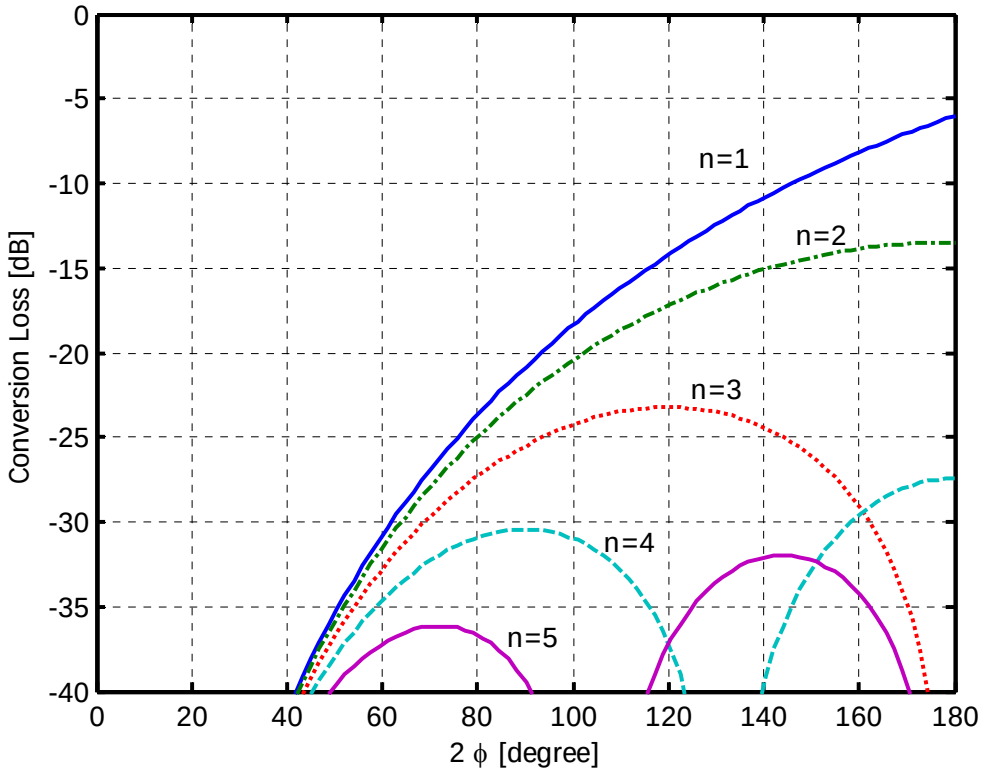


Fig. 4.3. Conversion loss of a bias controlled frequency multiplier as a function of conduction angle.

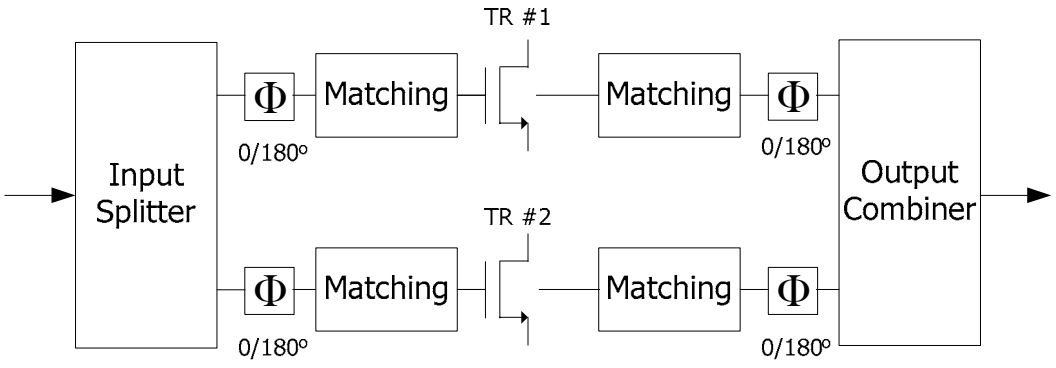


Fig. 4.4. Diagram of input and output phasing to switch between an amplifier and a frequency doubler.

Table 5. Input and output phase shifts for the amplifier mode and the frequency doubler mode.

MODE	TR#	Input Stage Phase Shift	Amplifier Phase Shift	Output Stage Phase Shift	Phase Shift Difference btw TR #1 and #2
Amplifier -1 (Push-Pull)	1	0°	180°	180°	0°
	2	180°	180°	0°	
Amplifier -2 (In-Phase)	1	0°	180°	180°	0°
	2	0°	180°	180°	
Doubler (Class B)	1	0°	180°	0°	180°
	2	180°	180°	0°	

Therefore, for dual-mode operation, input phasing might be reconfigured using a switch and a fixed-phase shifter in combination with gate-source biasing to select between the PA-mode amplification and the doubler-mode frequency multiplication. Fig. 4.5 shows the block diagram for a dual-mode transmitter.

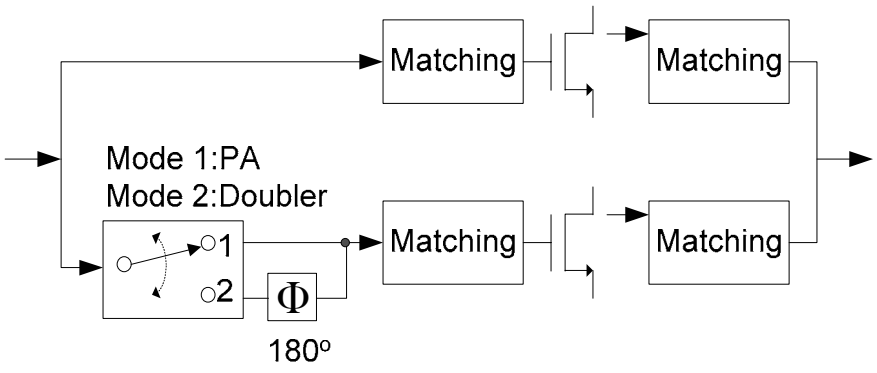


Fig. 4.5. Simplified schematic of an active, dual-band transmitter.

When the switch selects “Mode 1,” and transistors are biased for class-AB operation, the system is working as an in-phase combined amplifier. However, in doubler mode, the transistors are biased for class-B operation, and the switch selects “Mode 2” in which an additional 180° phase shift is given to the lower transistor path. This configuration is intended to generate maximum even harmonics for a frequency doubler with minimal conversion loss.

The output harmonic currents can be calculated from an expansion of (4.8), resulting in (4.10). Fig. 4.6 shows the current waveform with the conduction angle 2ϕ from this push-push type configuration.

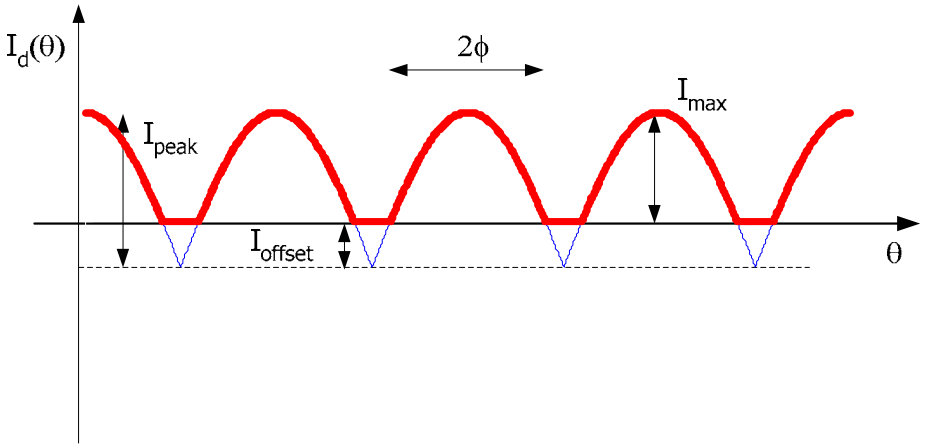


Fig. 4.6. Current waveform of push-push type harmonic generator.

$$I_{d,n}(\phi) = I_{peak} f_n(\phi)$$
$$= \left\{ \begin{array}{ll} 2\frac{I_{peak}}{\pi}\left\{\left(\frac{1}{n+1}-\frac{1}{n}\right)\sin[(n+1)\phi]+\left(\frac{1}{n-1}-\frac{1}{n}\right)\sin[(n-1)\phi]\right\} & : n \text{ even} \\ 0 & : n \text{ odd} \end{array} \right\}. \quad (4.10)$$

In this equation, the maximum second harmonic current happens when the conduction angle is 180°, and thus the system shows similar nonlinear transconductance of a full-wave rectifier. For comparison, the harmonic generation result of a push-pull waveform is shown in Fig. 4.7, and its harmonic currents are represented in (4.11).

$$I_{d,n}(\phi) = I_{peak} f_n(\phi)$$
$$= \left\{ \begin{array}{ll} \frac{1}{\pi}\{2\phi - \sin(2\phi)\} & : n = 1 \\ 2\frac{I_{peak}}{\pi}\left\{\left(\frac{1}{n+1}-\frac{1}{n}\right)\sin[(n+1)\phi]+\left(\frac{1}{n-1}-\frac{1}{n}\right)\sin[(n-1)\phi]\right\} & : n \text{ odd} \\ 0 & : n \text{ even} \end{array} \right\}. \quad (4.11)$$

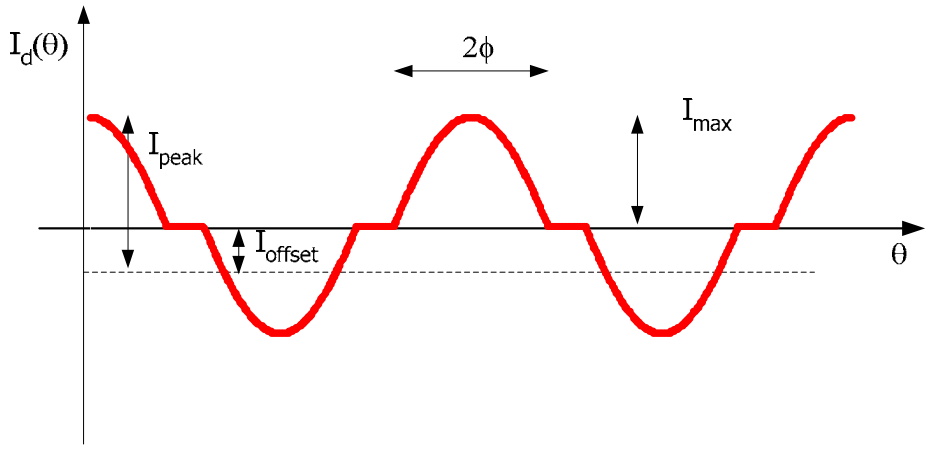


Fig. 4.7. Current waveform of push-pull type harmonic generator.

4.2.2 Output Combiner Design

The input matching circuit is chosen for conjugate matching at the fundamental frequency, and this matching is also valid for the doubler mode because the input frequency is the same for both modes. For output matching, however, because the output signal can be either at the fundamental frequency or at the second harmonic, the output matching circuit should have a low-Q topology. This will provide a wide bandwidth while maintaining the load-pull matching conditions to maximize the output current swings in both modes. This requirement can be achieved by designing a bi-tuned output combiner, which is explained herein.

For active devices, and especially for a dual-mode frequency doubler operating at the fundamental frequency and its second harmonic, the optimum impedances differ for maximum power at the fundamental frequency and at its second harmonic. The optimum impedance for n^{th} harmonic is given by the drain voltage and the harmonic drain current.

$$R_{L,n,opt} = \frac{V_{\max} - V_{\min}}{I_{d,n}} . \tag{4.12}$$

Because of the reduced conduction angle, the harmonic output current is normally less than the fundamental output current, so the optimum impedance in a frequency multiplier is greater than that for a regular PA. For this reason, when using a dual-mode frequency doubler, it is necessary to match those optimum impedance conditions for the fundamental signal and its second harmonic.

Based on an ordinary Wilkinson combiner, a bi-tuned combiner can be designed to meet the optimum load-line conditions for the fundamental and the second harmonic signals when the system consists of in-phase amplifiers. In the fundamental PA mode operation, the bi-tuned combiner puts together the power from two in-phased amplifiers with isolation as if it were a Wilkinson combiner. However, the device is working as a T-junction combiner in the doubler mode but with a different value of optimum load impedance for minimal power reflection. The isolation at the fundamental frequency is controlled by a resistance, which can also control the imbalance-rejection between two paths. In addition to the use of this device for a dual-mode amplifier, there may be opportunities for regular PAs to require that the second harmonic termination not be just grounded or open circuited but of any specific value. Therefore, although more investigation is required, the device may be used in a regular PA circuit as purposes dictate to provide a harmonic termination for the second harmonic. Designing the bi-tuned combiner starts with the ordinary Wilkinson combiner at the fundamental frequency f_1 as shown in Fig. 4.8.

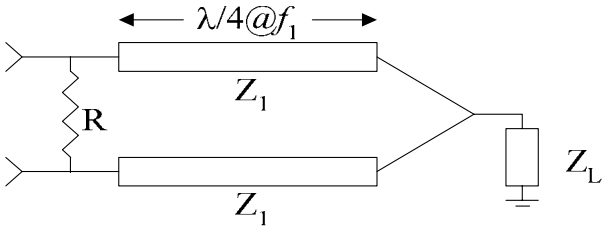


Fig. 4.8. Ordinary Wilkinson power combiner.

Given the bias voltage range and the output current, define the optimum impedances for the fundamental-mode and the frequency-doubler mode operation as $R_{opt,f1}$ and $R_{opt,f2}$. Then, along with the assumption that two PAs are in-phase, even-mode operation in the frequency-doubler mode is analyzed, and the circuit for this situation is presented below.

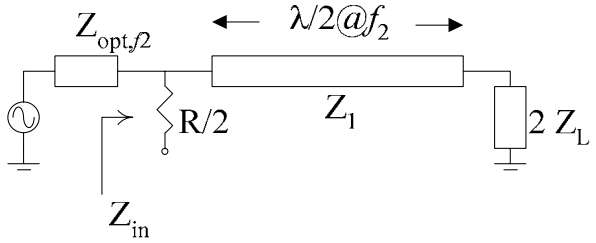


Fig. 4.9. Even-order circuit of the output combiner at the second harmonic.

The input impedance seen from the source impedance can be calculated from the transmission line formula [70].

$$Z_{in} = Z_1 \frac{Z_L + jZ_1 \tan \beta l}{Z_1 + jZ_L \tan \beta l}, \tag{4.13}$$

where Z_1 is the characteristic impedance of the transmission line, and Z_L is the load impedance connected to the transmission line. In this circuit, the load impedance is twice the original value for the even-order analysis, and the electrical length of the transmission line is one half the wavelength while it is one quarter of the wavelength at

the fundamental frequency. As such, if we assume a real valued Z_L, the input impedance looking into the device is simplified to twice the load impedance, regardless of the characteristic impedance of the transmission line. Hence, the load impedance can be chosen to meet the optimum impedance condition for zero reflection at the input port.

$$Z_{opt,f2} = Z_{in} = Z_1 \frac{2Z_L + jZ_1 \tan \pi}{Z_1 + j2Z_L \tan \pi} = 2Z_L . \tag{4.14}$$

Therefore,

$$Z_L = Z_{opt,f2} / 2 . \tag{4.15}$$

For the fundamental mode matching in Fig. 4.10, similar even-mode circuit analysis is used; however, the load impedance and the characteristic impedance of the transmission line affect the input impedance as below.

$$Z_{opt,f1} = Z_{in} = Z_1 \frac{2Z_L + jZ_1 \tan \frac{\pi}{2}}{Z_1 + j2Z_L \tan \frac{\pi}{2}} = \frac{Z_1^2}{2Z_L} . \tag{4.16}$$

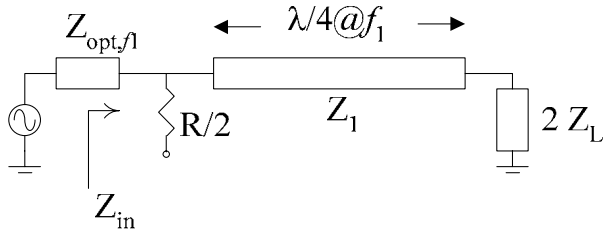


Fig. 4.10. Even-order circuit of the output combiner at the fundamental frequency.

In this equation, we have Z_L already fixed in (4.15) while Z_1 can be chosen to control Z_{in} for the ideal matching of Z_{in} to $Z_{opt,f1}$ as

$$Z_1 = \sqrt{2Z_L \cdot Z_{opt,f1}} = \sqrt{Z_{opt,f2} \cdot Z_{opt,f1}} \,. \tag{4.17}$$

Fig. 4.11 shows the circuit in odd-mode operation for the fundamental frequency signal. In this case, the input impedance is equivalent to *R*/2, and thus it is possible to manipulate the impedance seen from the odd-mode source so that we can control the amount of odd-mode signal reflection at the device input. The isolation of the even-mode signal in the fundamental mode is also controlled by this resistor. For the second harmonic in odd-mode, the input port is equivalent to being grounded, as depicted in Fig. 4.12.

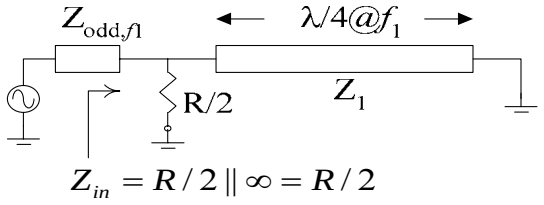


Fig. 4.11. Odd-order circuit of the output combiner at the fundamental frequency.

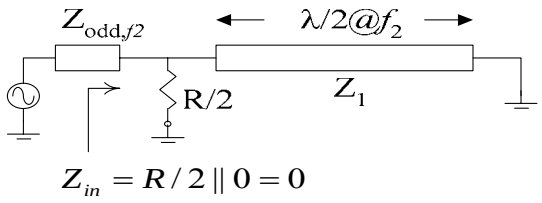


Fig. 4.12. Odd-order circuit of the output combiner at the second harmonic.

Since the maximum current of the second harmonic differs from the current of the fundamental, the load-lines must be set to extract maximum power whether the device is in the fundamental amplifier mode or in the doubler mode. As shown in this section, it is feasible to match output load impedances for the fundamental signal and its second harmonic independently when the dual-mode frequency doubler is designed with in-phase amplifiers.

4.2.3 Simulation

In order to verify the idea of the dual-mode device, the designed dual-mode frequency doubler was simulated by the harmonic balance simulation in ADS from Agilent. The transistor used for the simulation was Agilent's ATF-54143. The simulations were performed for two different topologies: the first topology is for an ideal case in which single-pole double-throw (SPDT) switches at the output of the transistors provide ideal phase changes between two signal paths for the amplifier and doubler modes. As expected, the performance of the unwanted harmonic cancellation was successful as well as the gain and efficiency in both modes. With an input frequency of 900 MHz, the gain

in the fundamental mode was around 20 dB, whereas the doubler mode showed a gain of 12 dB. Because of this gain drop, the power added efficiency (PAE) of the device for the doubler mode was around 35%, and the maximum PAE of the fundamental mode was 65%. A schematic for the simulation is shown in Fig. 4.13; Fig. 4.14 through Fig. 4.17 represent simulation results of the fundamental mode and the frequency doubler mode of the device.

Although the simulation shows satisfactory results, this architecture has the SPDT switches at the output of the transistors, which is not a desirable location in terms of additional loss and distortion. Hence, the second topology has the switches at the input of the transistors, and this location is adopted for the implementation.

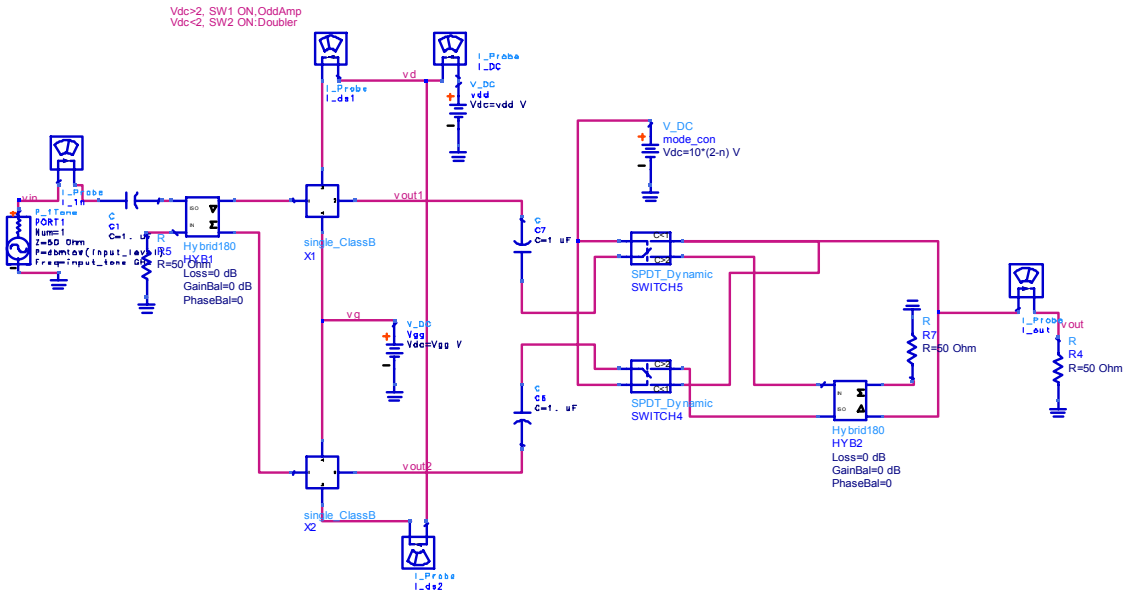


Fig. 4.13. Schematic of the active dual-mode frequency doubler with SPDT switches at the output ports of transistors.

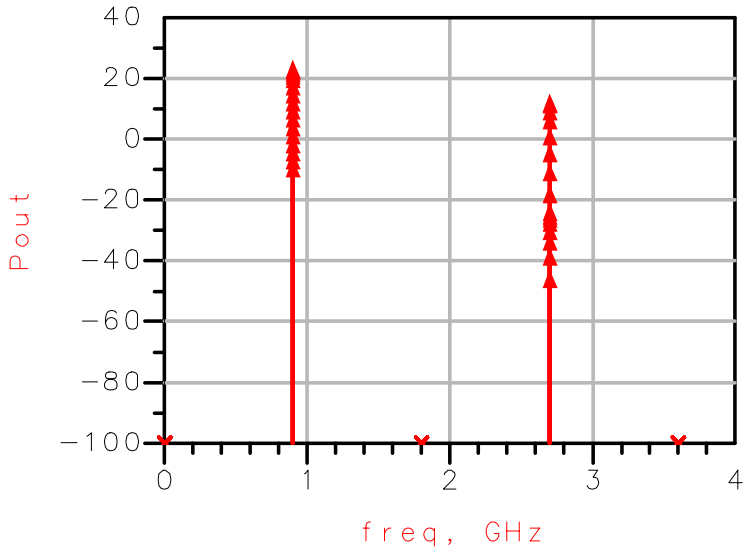


Fig. 4.14. Spectrum output of the amplifier mode operation with input power sweep.

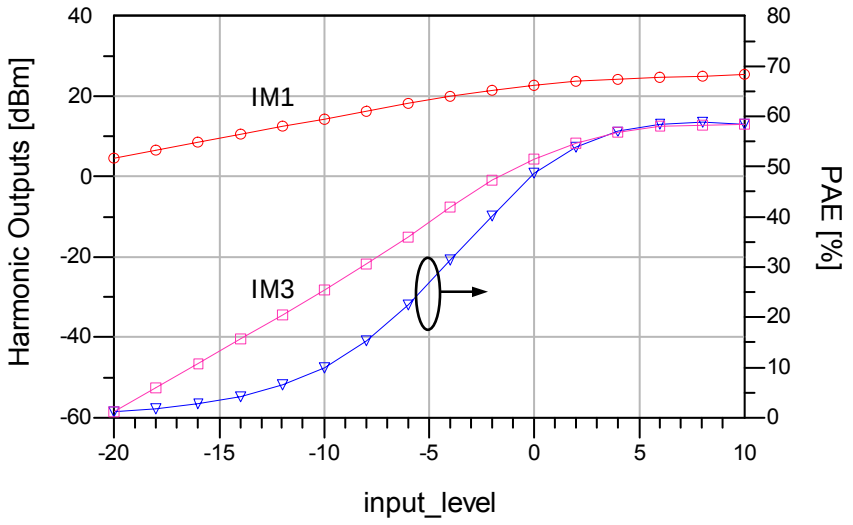


Fig. 4.15. Simulation result of amplifier mode operation: transistors are in-phase, Class-AB modes (V_{cc}=3 V, V_{gg} = 0.52 V).

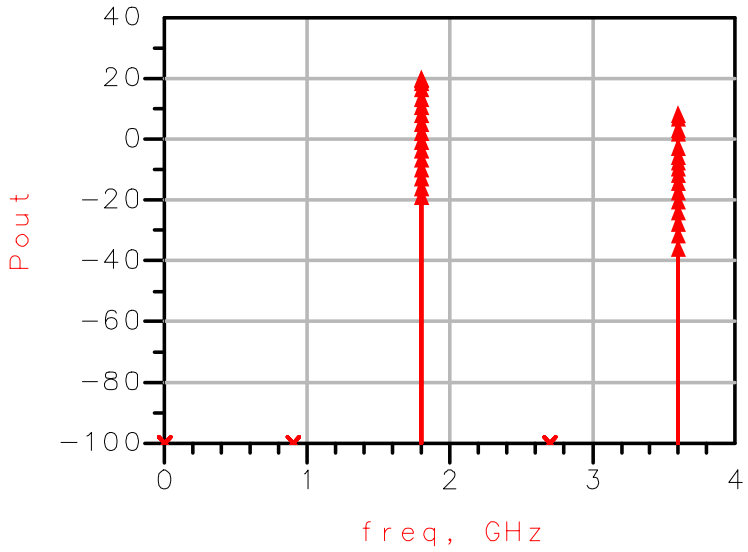


Fig. 4.16. Spectrum output of the doubler mode operation with input power sweep.

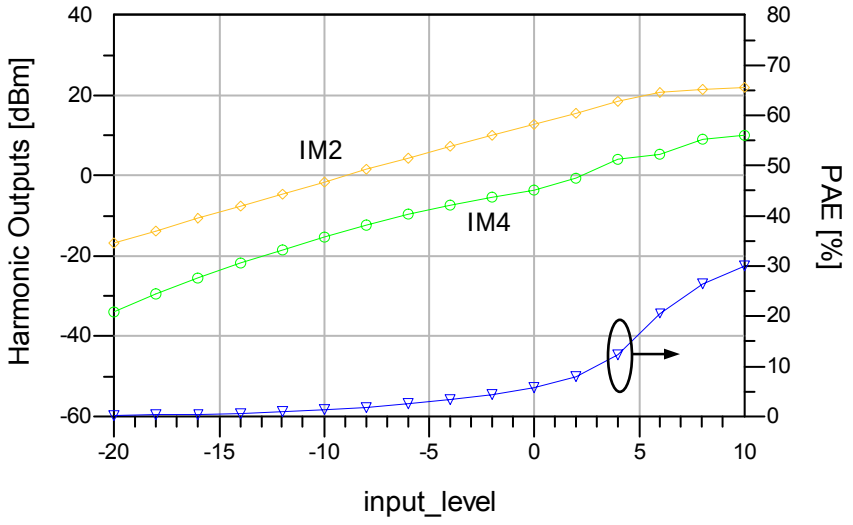


Fig. 4.17. Simulation result of doubler mode operation: transistors are push-push, Class-B modes (V_{cc}=3 V, V_{gg} = 0.32 V).

Based on this simulation, the actual dual-mode system with digital predistorter was also simulated in conjunction with the ADS and Matlab. The time-domain envelope simulation was performed in ADS but the digital data processing for predistortion was done in Matlab.

Because the transfer function with frequency multiplication includes higher order components, the implementation of the predistorter with polynomial inverse function in most cases finds less favor than the look-up table (LUT) method. This preference exists even though both performed almost equally for predistortion of a passive frequency doubler and tripler [12]. For this reason, the predistorter applied to this device was implemented with LUTs for magnitude and phase correction. The test signal was an IS-95B signal, which has a peak-to-average power ratio (PAPR) of 7 dB. Fig. 4.18 shows the simulation result of the system with digital predistorter. In this graph, the adjacent-channel power-ratio (ACPR) improved up to 45 dBc, whereas it was 20 dBc without the predistortion applied. The predistortion result applied to the fundamental mode amplifier is excluded from this work because its background theory and performance are widely published in the literature [48]-[50], [71]-[74].

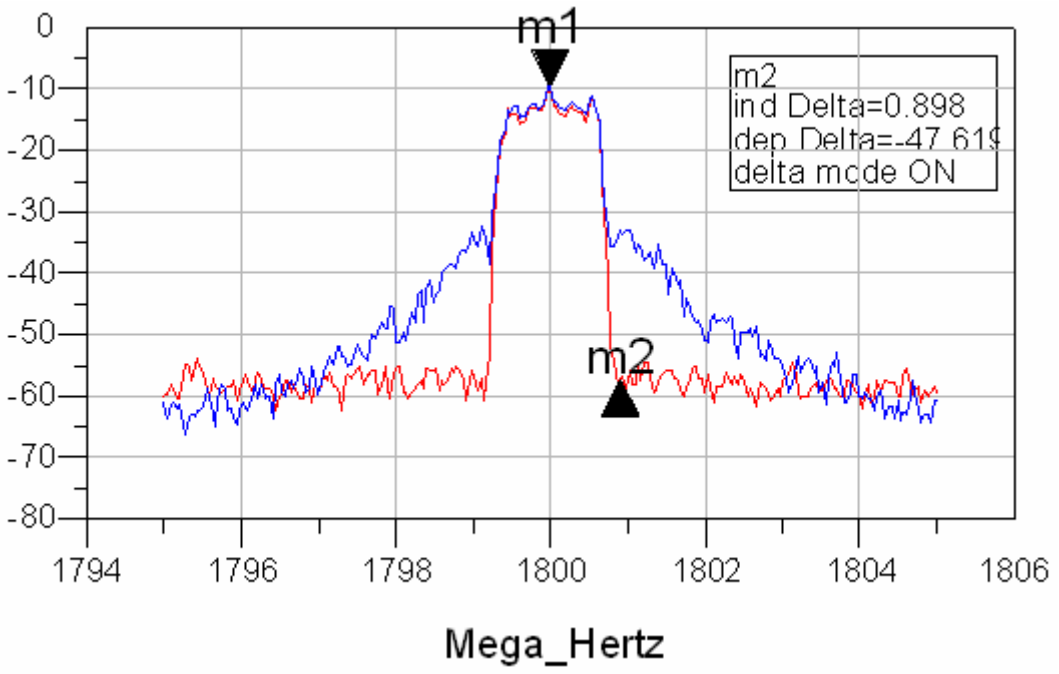


Fig. 4.18. Simulated predistortion result of the dual-mode device in frequency-doubler mode with IS-95B input at 900 MHz.

4.2.4 Dual-Mode Amplifier System Design

Fig. 4.19 shows the overall circuit for the dual-mode frequency doubler. The circuit is designed to operate at the fundamental frequency of 900 MHz, and thus the second harmonic is 1800 MHz. For selectable input-phase switching in a path, a SPDT switch and a 180° delay line at 900 MHz were placed in front of the input port of a PA in such way that the SPDT switch can bypass the delay line. In the PA-mode operation, the signal is fed into the PAs of both paths in-phase, whereas in doubler mode operation one of the signal paths goes through the 180° phase shifter. As a consequence, the odd-order signal is canceled out at the output of PAs. In addition, gate-source bias voltage should be used to maximize the second harmonic along with the optimal drain-source voltage,

when the PAs are operating in class-B mode, for maximized second harmonic generation. These bias points for each mode can be selected through DC bias measurements.

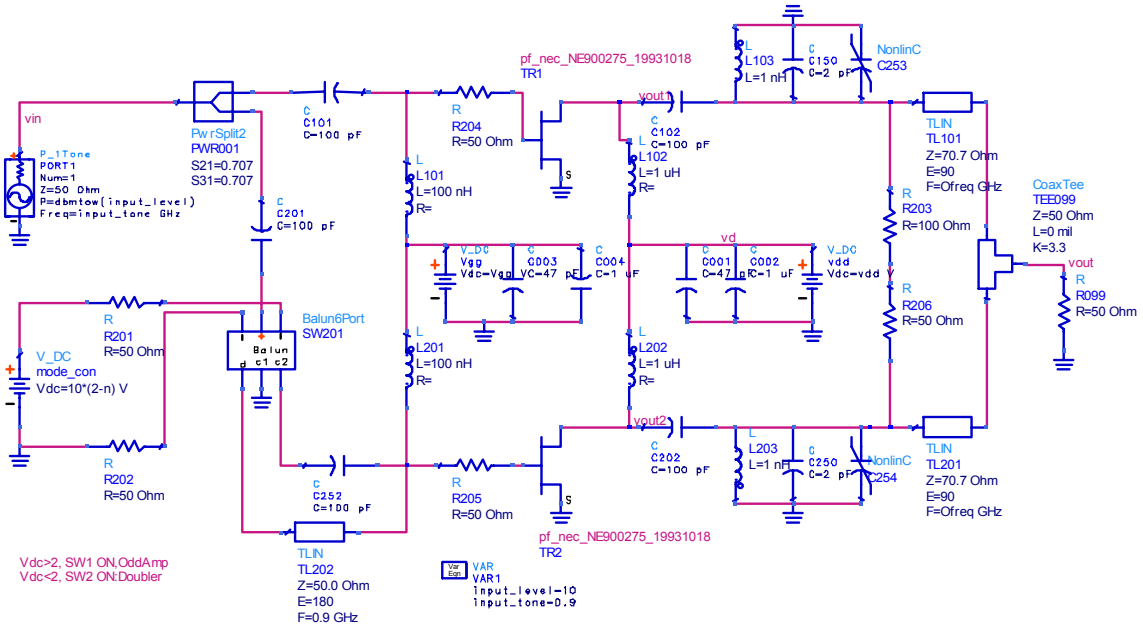


Fig. 4.19. Schematic of the dual-mode power amplifier.

The output tuning circuit is mainly intended to provide undesired harmonic reflection, which is possible by the careful tuning of the resonating frequency at the fundamental or at the second harmonic. This may be done by changing the shunt inductance or by carefully optimizing the varactor capacitance with a control voltage. In the realization of the circuit, however, this variable tuning was performed manually by putting the shunt inductance in or taking it out instead of electronically controlling the varactor diode.

This procedure was followed simply because of the availability of the diode, although the implementation of electronic control of the varactor diode is not expected to be difficult.

4.3 VARACTOR DOUBLER

A nonlinear reactance, such as a varactor diode, can be used to translate RF power from one frequency to another, theoretically with 100% efficiency. In contrast, the best possible efficiency of a nonlinear resistance frequency multiplier is inversely proportional to the square of the harmonic number [75]. The main drawback of reactive multipliers is that they have much smaller bandwidths than frequency multipliers that are based on a nonlinear resistance. However, for a reactive frequency multiplier, it is possible to get high efficiency over relative bandwidths of 3-5%, which are acceptable for modulation formats used in wireless systems. Fig. 4.20 and Fig. 4.21 show two lumped-element model designs, respectively, for lower and higher output powers and are syntheses of ideas taken from [76] and [77].

There is a classic theory about the design of varactor frequency multipliers [76], but this theory assumes that the only loss mechanism in the circuit is the series resistance of the diode. However, our simulation studies show that for varactor doublers fabricated with microstrip resonators for cost and space savings, the dielectric loss and the copper loss cause efficiency degradation at least as great as that from the diode's series resistance. Hence, some optimization of the classical design is necessary.

In Fig. 4.20, energy from the source at frequency f is converted to energy at frequency $2f$ and dissipated across the output load Z_L. The "trap" C1/L1 is parallel resonant at $3f$,

hence no third-harmonic current can flow through the varactor diode. The input circuit consisting of L5, C3, and L3 are chosen to be series resonant at frequency *f*, hence a large current can flow through the diode to ground at this frequency.

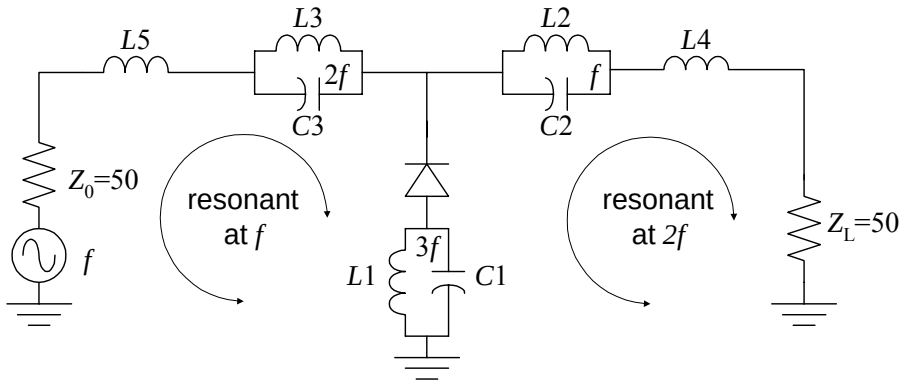


Fig. 4.20. Schematic of the lower power varactor-diode frequency doubler (L-doubler).

Moreover, C3/L3 is parallel resonant at 2*f* so that the second-harmonic current evoked by the diode cannot flow back to the input circuit. In a similar fashion, L4, C2, and L2 are chosen to be series resonant at the output frequency 2*f*, and drive a current at this frequency through Z_L. The parallel resonance of L2/C2 at frequency *f* prevents input current from flowing through the load. Such a current flow would be undesirable from a standpoint of spectral purity of the output, as well as a waste of input power.

With this lumped-element design, the resonant components were replaced by microstrip lines, and this design was fabricated and tested. This circuit was simulated with Agilent ADS using a surface-mount SMV1405 diode from Skyworks. The practical design also requires a bias voltage across the varactor.

The second design in Fig. 4.21 uses four diodes in a bridge configuration, which achieves higher output power than the single-diode configuration because the current is shared among four diodes. In addition, the design uses balanced rather than tuned diplexers to separate the drive signal from the double output, eliminating another source of loss.

With reference to Fig. 4.21, the network L1/C1 is parallel resonant at the third harmonic (2.85 GHz), so no current flows through the diodes at this frequency. Anti-phase drive at 950 MHz is applied to the two sides of the bridge, but networks L2a/C2a and L2b/C2b parallel resonate at 1900 MHz preventing the source resistance of the two driving sources from loading the bridge at the output frequency. Finally, the inductor L3 series resonates the diode network at 1900 MHz so that a large output current can flow through the load. Current at 950 MHz does not flow into the load because of the circuit balance. In practice, the design is realized with half-wave and quarter-wave lines to achieve series or parallel resonances; varactor diodes are BB833 from DigiKey; bias is not shown.

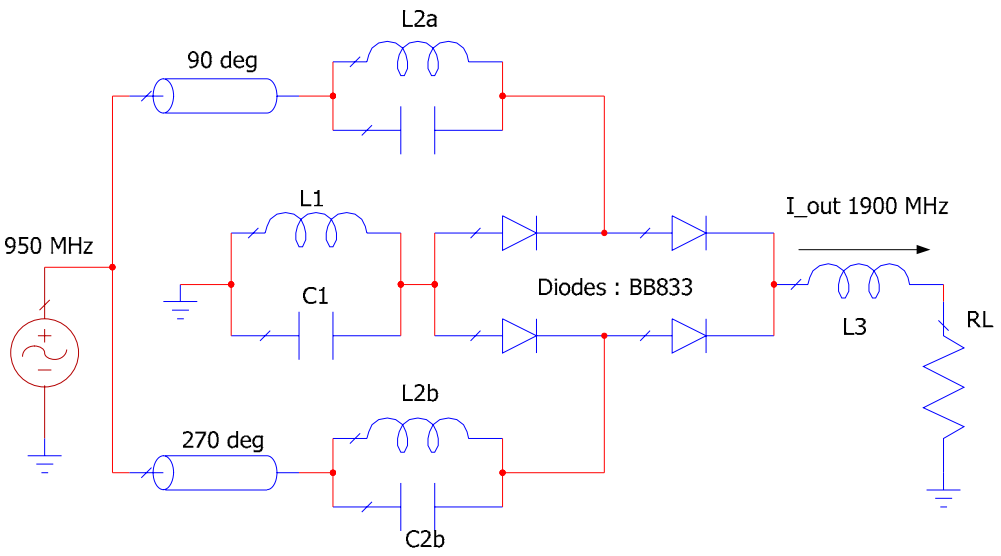


Fig. 4.21. Schematic of the higher power varactor-diode frequency doubler (H-doubler).

Based on these two reactive frequency doublers, the second dual-mode transmitter can be implemented by adding a SPDT switch at the output of a PA of the fundamental frequency. This RF switch can bypass the frequency doubler for PA-mode operation, and route to the doubler for doubler-mode operation. Fig. 4.22 shows the block diagram of this concept.

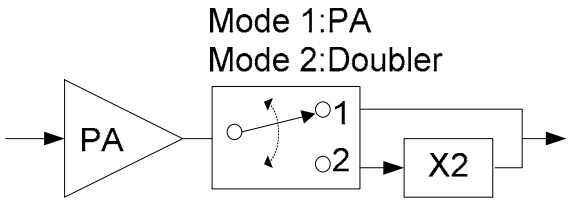


Fig. 4.22. Block diagram of a dual-mode transmitter with an SPDT switch at the output of a PA.

4.4 EXPERIMENTAL RESULTS

Two active dual-mode frequency doublers and two varactor frequency doublers were built by the author for the transmission of digital signals. The active doublers incorporate transistors for the realization of a PA with the dual-mode capability for 900 MHz and 1800 MHz transmission. Secondly, 1850 MHz signal generations with the two varactor-doublers were performed. In all, the system puts the predistorted IS-95B signal into the devices and, according to the operating mode, takes the output signal at the fundamental or second harmonic frequencies. The measured signal is downconverted, digitized, and analyzed in the baseband signal processing. Finally, a LUT based digital predistorter updates its coefficients and cancels out the nonlinearity as described in [12].

4.4.1 Active Dual-Mode Doublers

For the lower power active dual-mode doubler, referred to as doubler-I from here on, the Agilent's ATF-54314 was used for active components, and the architecture in Fig. 4.5 was implemented. In the fundamental-mode operation, the carrier frequency was 881.5 MHz, and the gain for class-AB operation was 9.7 dB when the input power was 0 dBm. In the frequency-doubler mode operation, the output signal was taken at 1763 MHz. The gain in this case was 10.2 dB at the input power of -1 dBm, and 7 dB when we backed off by 6 dB for the predistortion.

The higher power active doubler, doubler-II, was built with Sirenza's SHF-0289 GaAs HFET 1 Watt transistors, which have good high frequency capability showing relatively

low output capacitance, which is critical for harmonic generation. From the measurement of a single transistor and the simulation of the system with active devices of the same material, it was expected to have R_{opt} of 25 ohm at the fundamental frequency and 50 ohm at the second harmonic. The output bi-tuned power combiner was designed based on these values, and the other circuit values, including output-matching circuits, adopted the values from the characterization of a single-transistor measurement that was performed beforehand. Then, after the transistors and miscellaneous circuit-components are integrated into the system, these values were fine –tuned to improve performance still further. Fig. 4.23 represents the fabricated active, dual-mode frequency doubler with an operation-mode control circuit and the pre-described output combiner.

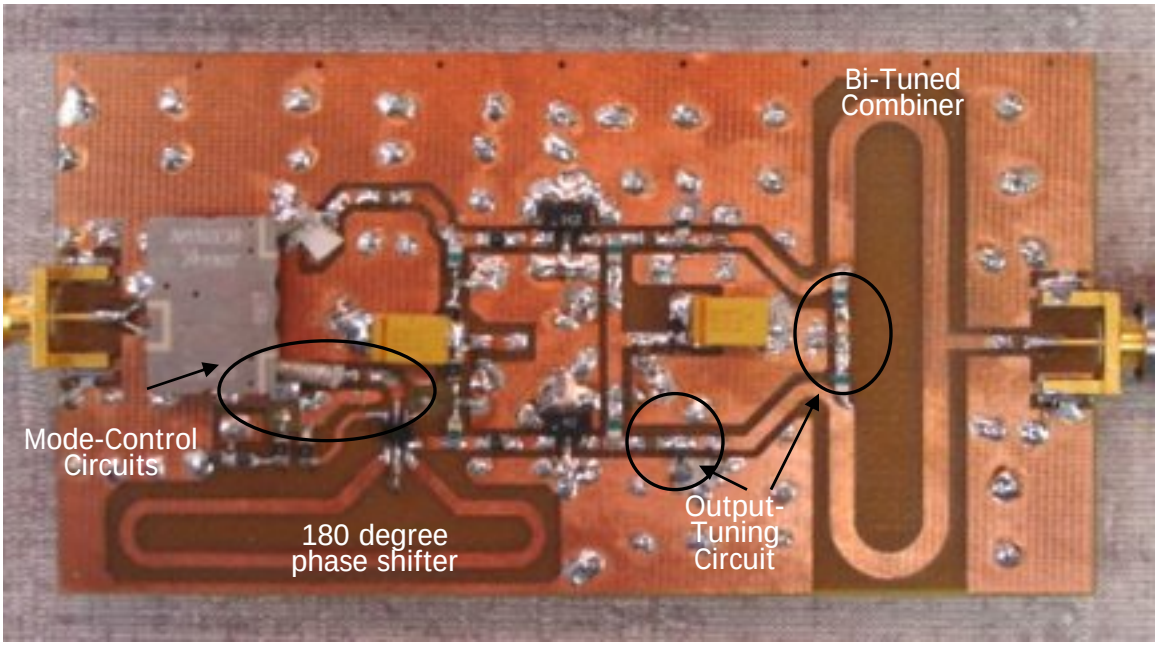
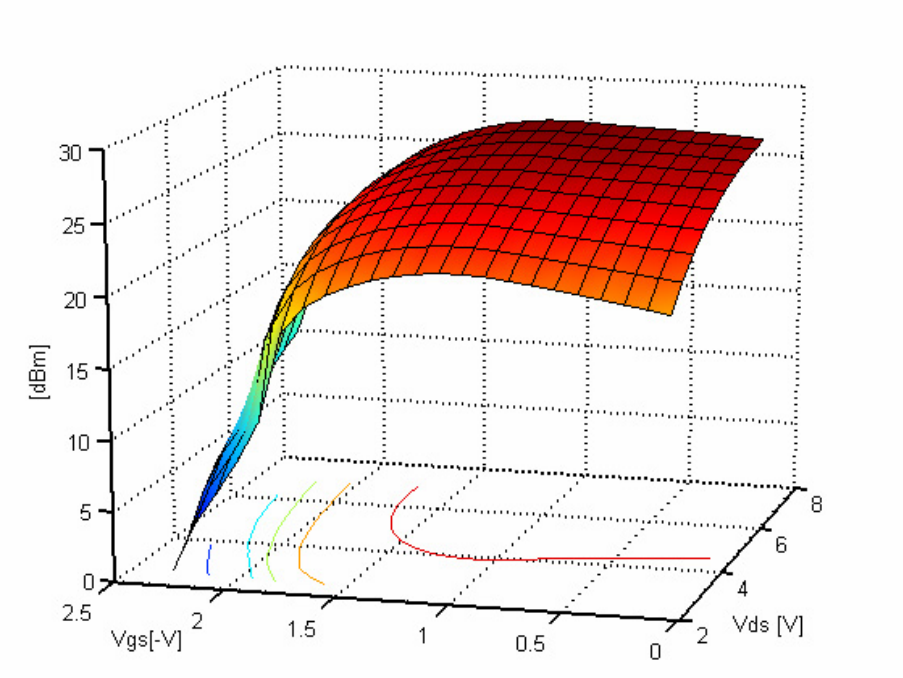


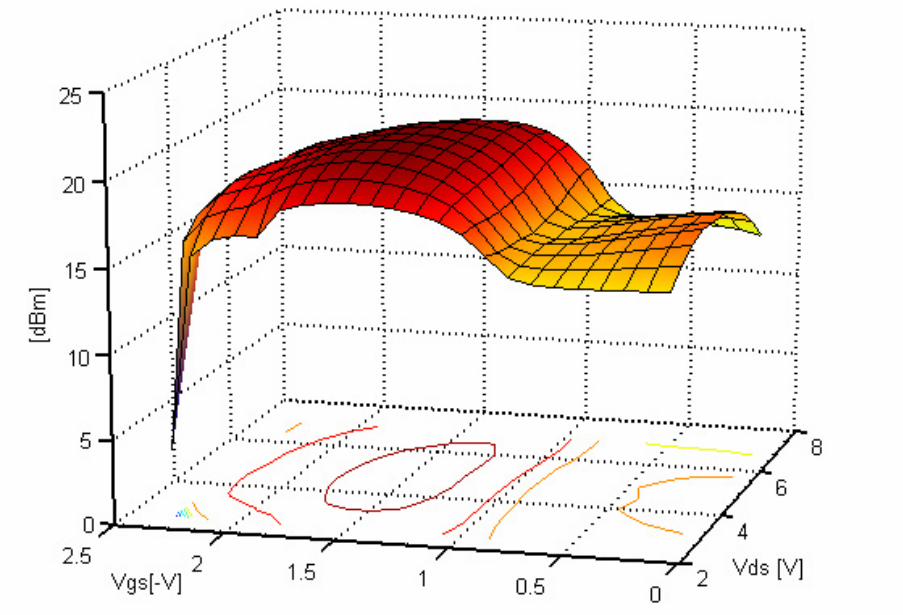
Fig. 4.23. Assembled active dual-mode frequency doubler with in-phase 1 W PAs (doubler-II).

This doubler-II was measured by ranges of drain and gate voltages, and showed outstanding results for the fundamental mode and the doubler mode operations, which are shown in Fig. 4.24 (a) and (b), respectively. As shown in these figures, the maximum powers were 28 dBm and 21.8 dBm for the amplifier mode and doubler mode, respectively.

Fig. 4.25 (a) and (b) show drain efficiencies for both modes. The maximum efficiency was 29.1% in the fundamental mode, and 22.2% in the doubler mode. In addition, the power sweep results are shown in Fig. 4.26.

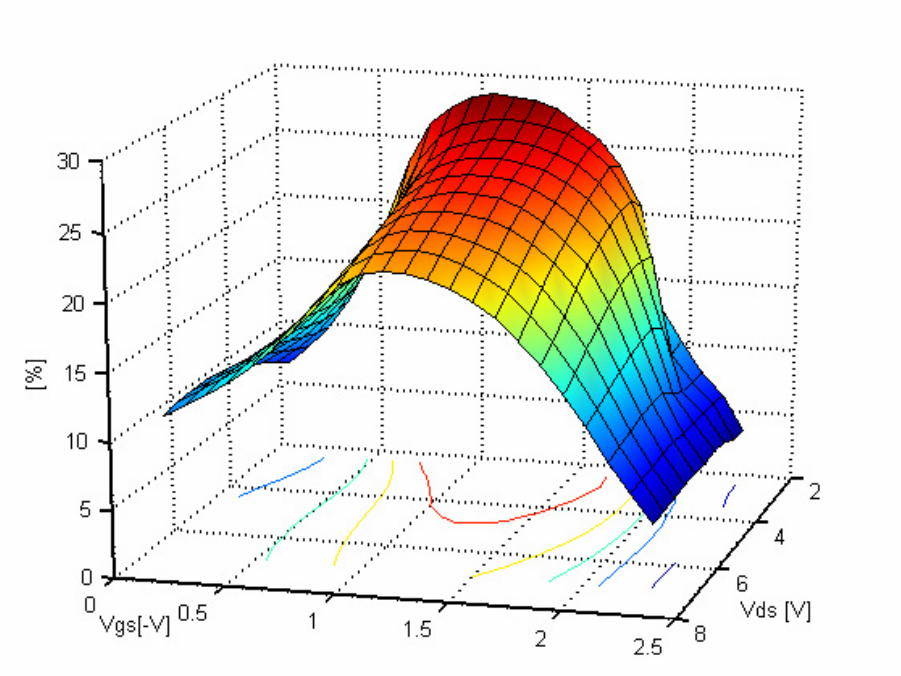


(a) $P_{out}@f_1$ (CW) for the amplifier mode operation over DC biases.

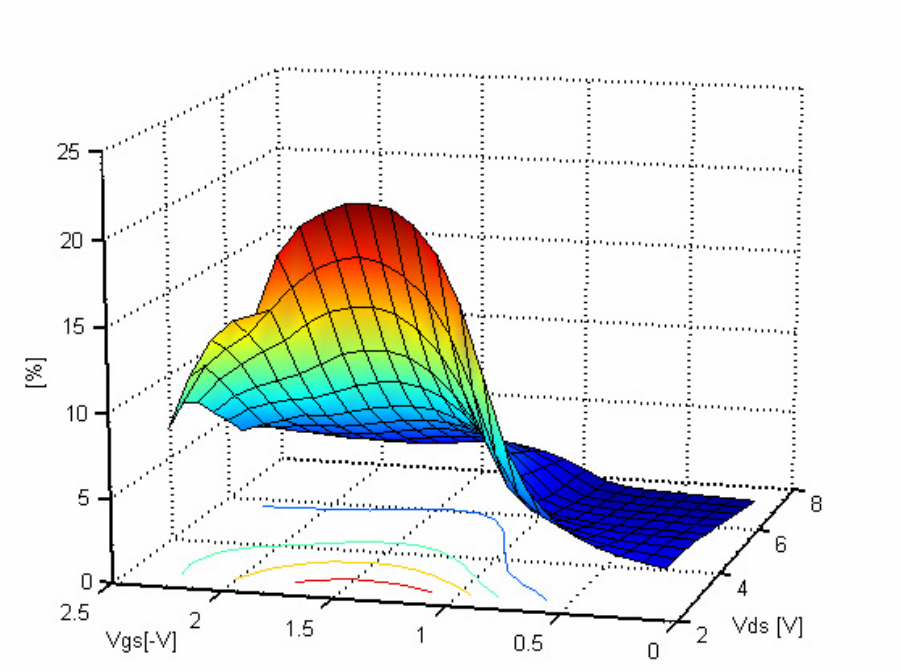


(b) $P_{out}@2f_1$ (CW) for the doubler mode operation over DC biases.

Fig. 4.24. Variation of output powers over DC biases (doubler-II).

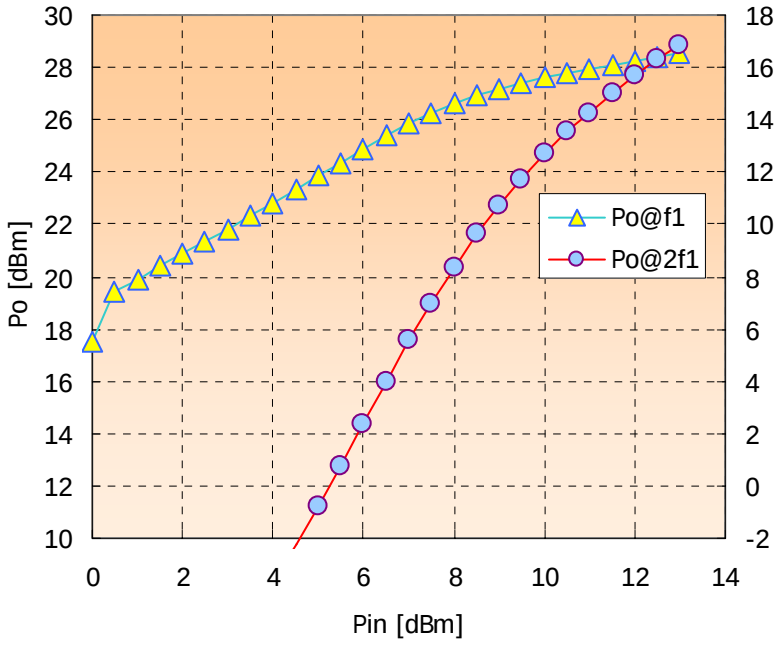


(a) Efficiency@f_1 (CW) for the amplifier mode operation over DC biases.

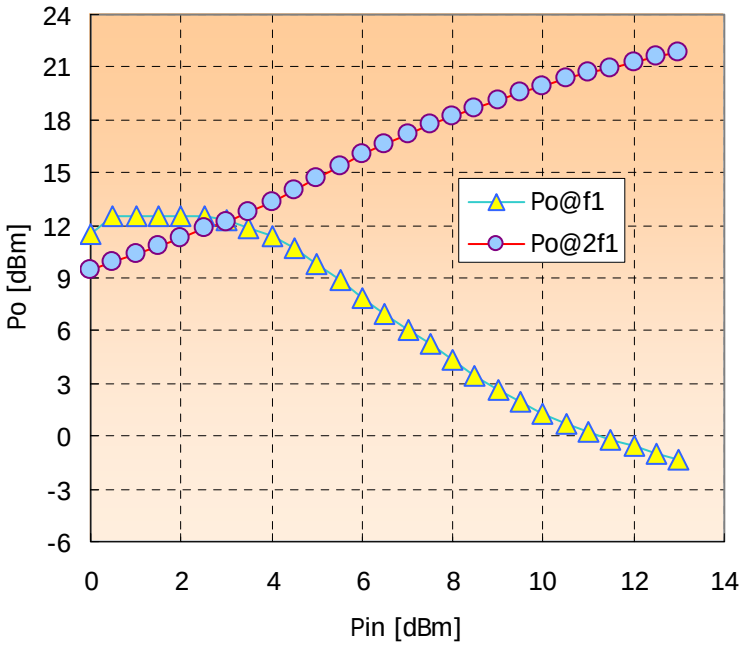


(b) Efficiency@$2f_1$ (CW) for the doubler mode operation over DC biases.

Fig. 4.25. Variation of Efficiencies over DC biases (doubler-II).



(a) In amplifier mode

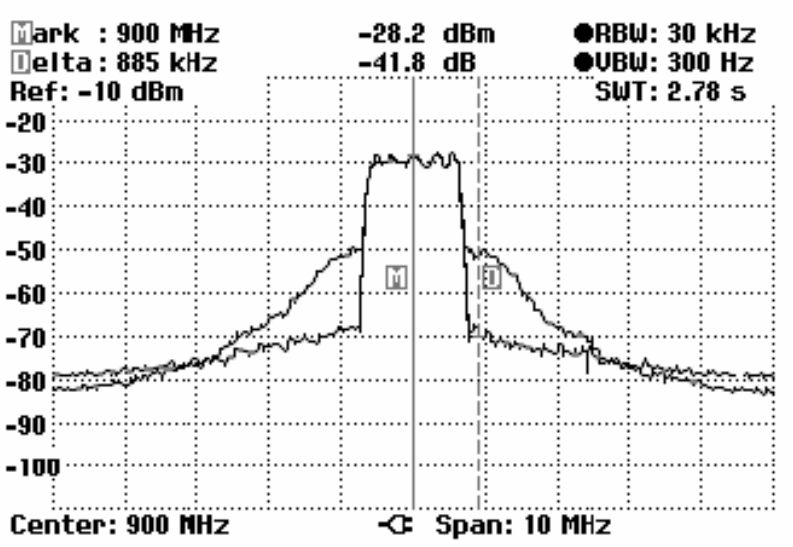


(b) In doubler mode

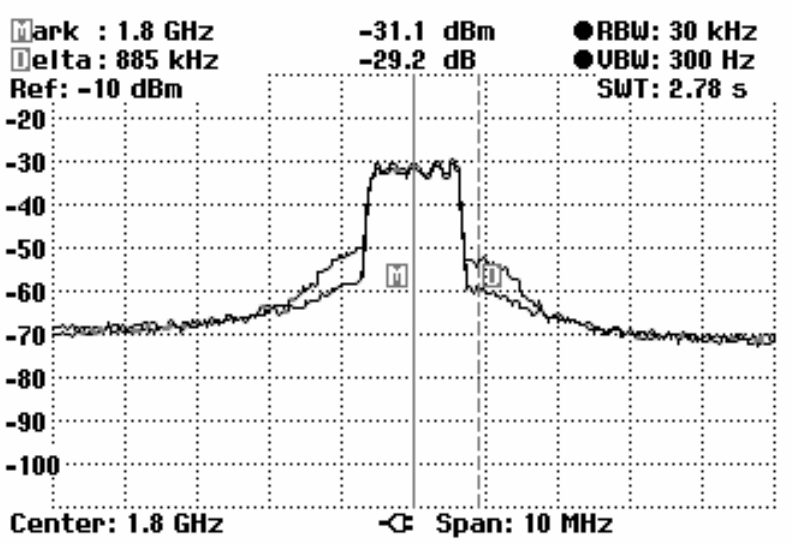
Fig. 4.26. Power sweep results of doubler-II in both modes.

For the predistortion of active doublers, the IS-95B signal at 881.5 MHz was applied with an LUT-based adaptive digital predistorter, and then the ACPR (the ratio of the interference power in 30 kHz bandwidth at an adjacent channel to the total signal power in 1250 kHz bandwidth) at 885 kHz offset was measured. In the case of doubler-I, the fundamental mode ACPR was -56.4 dBc/30 kHz. In comparison, the ACPR after predistortion in doubler mode was -48 dBc/30 kHz at 885 kHz offset, whereas it was -26 dBc/30 kHz without predistortion. Phase division of the input signal was applied for both cases. Although the output frequency of the doubler-mode was chosen at 1763 MHz, it can be easily changed to cover the 1800 MHz band that is used for PCS cellular communication.

In the case of doubler-II, the fundamental frequency and the second harmonic for the measurement were, respectively, 900 MHz, and 1800 MHz, and the predistortion results are shown in Fig. 4.27. The predistortion results are -58 dBc/30 kHz in amplifier mode, and -45.4 dBc/30 kHz in doubler mode. These measurements were taken at an output power of 21.8 dBm and 16.1 dBm, respectively, for the amplifier mode and doubler mode.



(a) Measured predistortion result of fundamental-mode operation. The output power was 21.8 dBm



(b) Measured predistortion result of doubler-mode operation. The output power was 16.1 dBm

Fig. 4.27. Measured predistortion results of both modes of the active, dual-band transmitter with the input signal of IS-95B at 900 MHz (doubler-II).

The bandwidth of doubler-II is mainly limited by the output combiner, which depends on microwave theories for the quarter-wavelength and half-wavelength transmission lines. Therefore, in case a wideband bi-tuned combiner is available either by higher order matching or by any optimization technique, a moderately wideband local synthesizer can successively generate the fundamental so that its second harmonic can fall into a desired frequency band. In Fig. 4.27, the noise floor is increased in doubler mode, where this phenomenon may be presumably contributed by the $20\log N$ as with any frequency multiplier, and by a nonlinear AM-PM conversion [21]. However, given that the system is linearized by an adaptive predistorter, it may be more appropriate that in doubler mode the memory effect is the second major contribution to the increase in the noise floor. The validity of this assumption can be verified by the existence of more asymmetry in the frequency domain in doubler mode than is present in the amplifier mode.

4.4.2 Varactor Frequency Doubler

For the low-power varactor doubler (L-doubler) measurements, the input frequency was set at 926 MHz with 15 dBm of power, and the output was measured at 1852 MHz, where the measured conversion loss was 3.3 dB. In the same way as with the active dual-mode frequency doubler, the digital baseband predistortion was applied to the IS-95B signal; Fig. 4.28 and Fig. 4.30 show the fabricated device and the predistortion results with and without the predistortion at a channel power of 9 dBm. In addition to the predistortion, phase division was applied in both cases because the output signal was not de-modulatable as a QPSK signal unless phase division was applied.

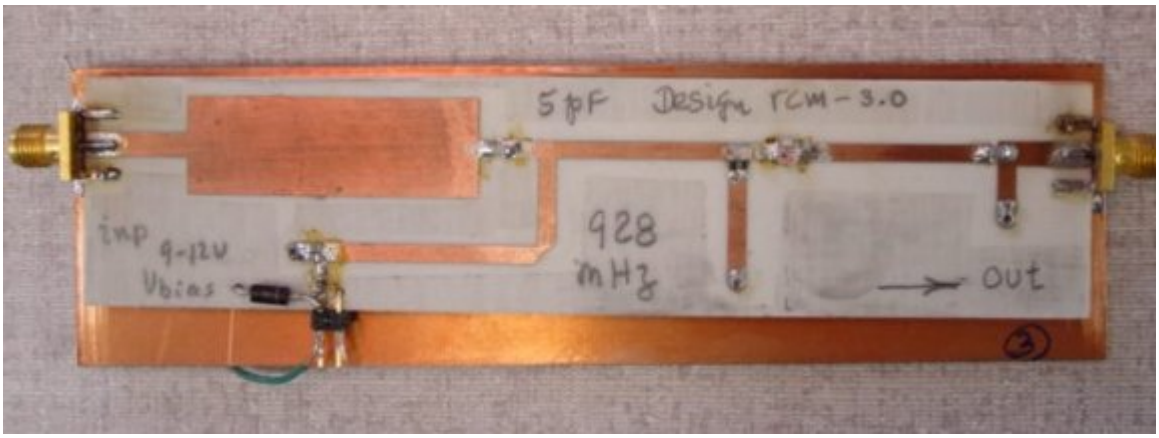


Fig. 4.28. Fabricated lower power varactor-diode frequency doubler (L-doubler).

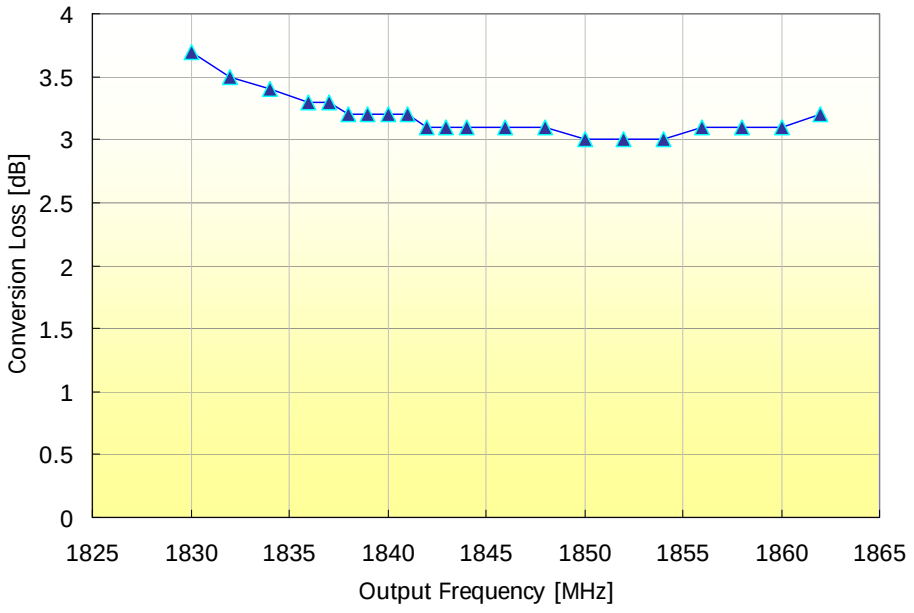


Fig. 4.29. Frequency response of the L-doubler.

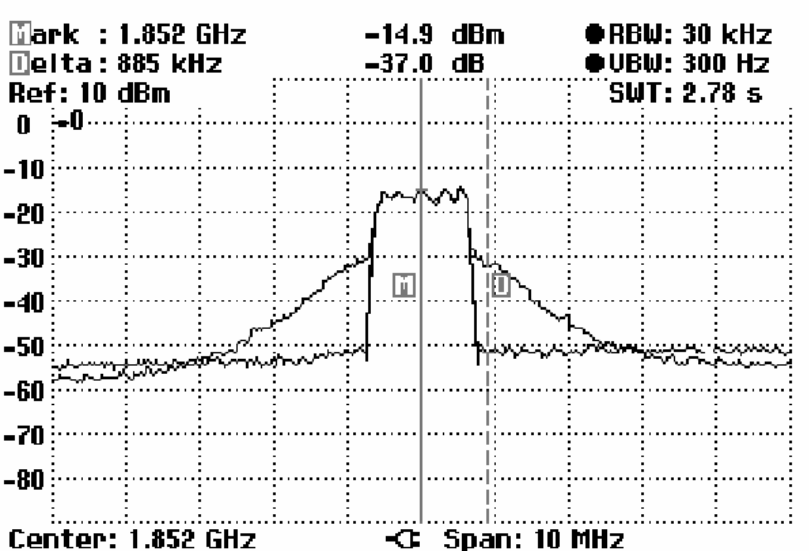


Fig. 4.30. Measured predistortion result of the L-doubler with the input signal of IS-95B at 926 MHz. The output power was +9 dBm.

For the high-power varactor doubler (H-doubler) measurements, the input frequency was set at 925 MHz with 25 dBm of maximum input power, and the output was measured at 1890 MHz, where the measured conversion loss was as low as 1.3 dB. Fig. 4.31 is a picture of the implemented device. As in the other cases, digital baseband predistortion with a IS-95B signal was applied. The results are shown in Fig. 4.32 for cases with and without the predistortion at a channel power of 19 dBm. The limitation on the dynamic range (DR) of the output signal is because of the limitation of the DR of the predistorted IS-95B source file and the 20log*N* increase in the noise floor. The power sweep results of the conversion loss and the predistortion performance are shown in Fig. 4.33.

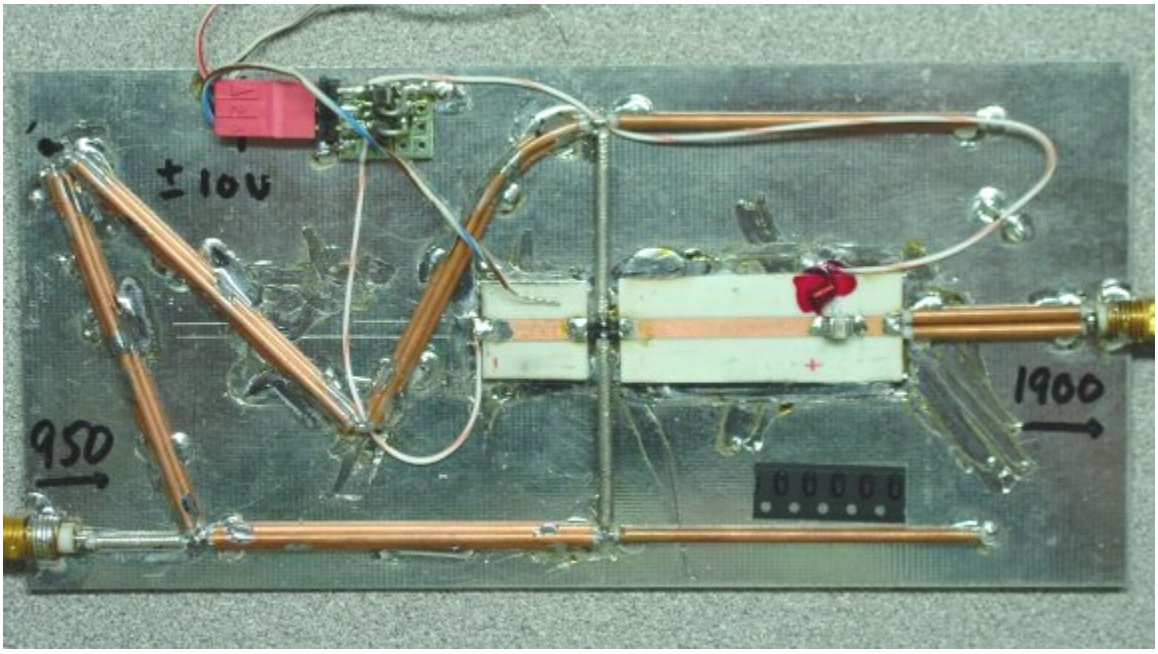


Fig. 4.31. Fabricated higher power varactor-diode frequency doubler (H-doubler).

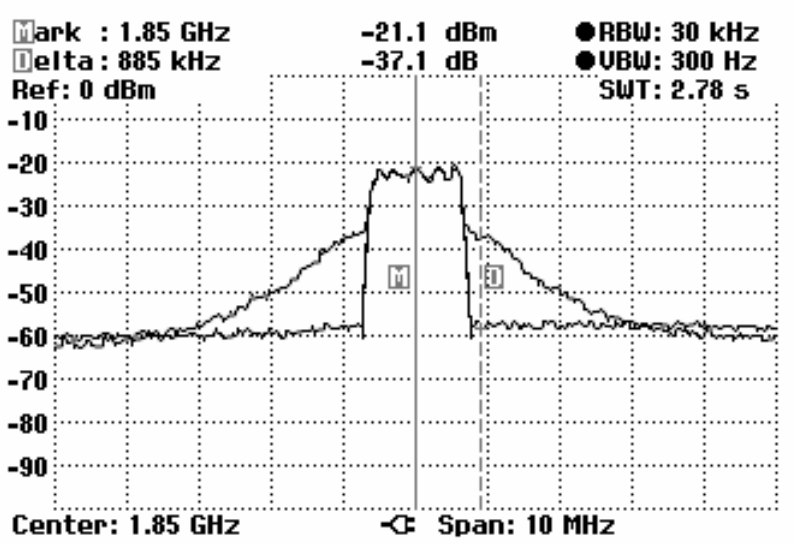


Fig. 4.32. Measured predistortion result of the H-doubler with the input signal of IS-95B at 925 MHz. The output power was +19 dBm.

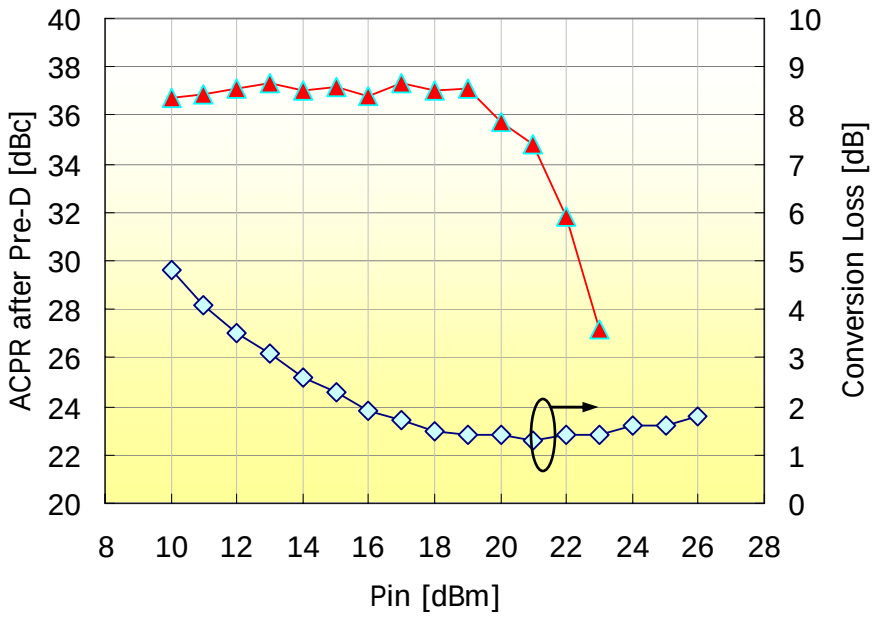


Fig. 4.33. ACPR improvements and conversion loss of H-doubler over the input power.

4.5 CONCLUSIONS

Two architectures for reconfigurable radios, especially for dual-band transmission systems, have been suggested and implemented with baseband digital predistortion for envelope-modulated digital signal transmissions. First, mode-switchable PAs were designed to amplify signals by proper control and biasing in a fundamental frequency or in the second harmonic frequency. To get the maximum output power at the desired frequencies for each mode, a specially designed output combiner and an input and output tuning circuit were suggested and implemented. Referring to the higher power device, doubler-II, the fabricated PA showed 28 dBm of maximum output power with input power of 10 dBm, and a maximum efficiency of 29.1% in fundamental mode, whereas

the numbers were 20.6 dBm and 22.2% in doubler mode. Digital predistortion applied to the device improved the ACPR of the IS-95B signal by 20 dB in the fundamental mode and by 8 dB in the doubler mode, achieving the final ACPR with appropriate output back-offs of 57.8 dBc/30 kHz and 45.2 dBc/30 kHz, respectively. The relatively low ACPR improvement in the doubler mode is presumably contributed by the increased noise floor from the phase noise multiplication and additional memory effect in this specific mode. Overall, the dual-mode PA proved the feasibility of the simplified architecture for a dual-band transmitter by requiring far fewer components than the conventional two-path dual-band transmitters.

Second, two varactor-diode frequency doublers were designed and built as well. These devices can be used either as plug-ins in a circuit after a power amplifier, or be bypassed using an RF switch for a desired output frequency. In the case of the higher power doubler (H-doubler), because the conversion loss of the device is extremely low up to 26 dBm of input power, its application to the dual-mode transmitter is promising when connected to an efficient PA. The resulting performance of the H-doubler with digital predistortion showed -53 dBc/30 kHz of ACPR at 1850 MHz with conversion loss of 1.5 dB, and the output power was 19 dBm.

Comparing the two ideas for dual-band transmitters, the active dual-mode amplifier can be considered the more feasible approach when optimized for higher power application; on the other hand, the varactor doubler approach showed better conversion efficiency, although it may introduce additional loss and distortion from a bypass switch.

CHAPTER 5

ADAPTIVE SUB-SAMPLING FEEDBACK IN PREDISTORTION SYSTEMS

5.1 INTRODUCTION

Because a PA's distortion characteristics may change in response to temperature, voltage, and aging, adaptive architectures are often employed to correct the linearization parameters to maintain optimum IMD correction. These correctives employ feedback circuits that sample input and output signals to calculate the best set of linearization parameters. As for the sampling process in the feedback circuits, it is often assumed that full Nyquist rate sampling must be used to properly reconstruct input and output waveforms to extract all PA distortion characteristics [78], [79]. Fig. 5.1 shows the block diagram of an adaptive predistorter.

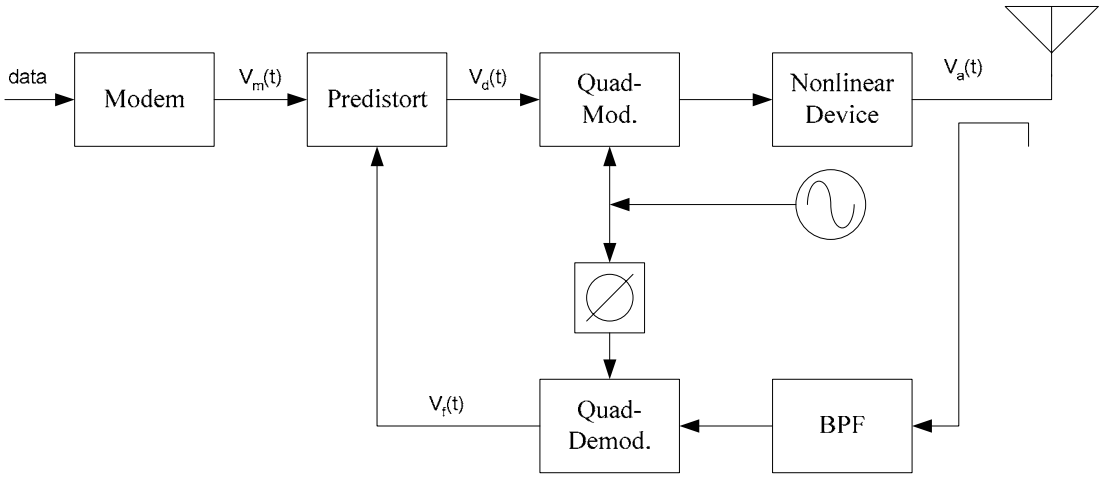


Fig. 5.1. Block diagram of a generic adaptive predistorter.

For multicarrier applications, full-rate sampling can become costly because the bandwidth of the signals often exceeds 30 MHz. Moreover, the PA output signal bandwidth is three to five times larger than the input signal bandwidth because of the spectral regrowth created by IMD. Thus, for many such applications, sample rates in excess of 300 Msps must be employed if alias-free signal reconstruction is desired. With the required resolution being 12 to 14 bits to obtain sufficient dynamic range, these high sampling rates pose significant challenges to the achievement of cost-effective adaptive predistortion systems. In an effort to ease this sampling requirement, harmonic sampling — also called under-sampling — was introduced, and its sampling criterion was established using the reciprocity of a band-limited signal in the discrete domain [15], [16], [80].

5.2 SUB-NYQUIST RATE SAMPLING THEORIES

5.2.1 Generic Idea for Sub-Nyquist Rate Sampling

This section introduces a new predistortion architecture whereby the LUT data may be obtained using sampling rates lower than the full Nyquist-rate sampling of the output signal. The concept rests on the fact that the distortion characteristics of a memoryless device may be identified using a set of independent samples from the input and output, regardless of when they have been taken as long as the number of samples is adequate to characterize the nonlinear distortion of the device.

Assuming that a nonlinear system is time-independent and invertible, then $x(t)$ and $y(t)$ — the input and output of the system — have a one-to-one nonlinear function $F(\ )$, which can be simply defined as below [81].

$$y(t) = F(x(t)), \tag{5.1}$$

and

$$y(t+\tau) = F(x(t+\tau)), \qquad \tau \neq 0. \tag{5.2}$$

Then, when we further assume that the system is memoryless, the input and output matching function $F(\ )$ is always maintained at any instant of t, which is obvious because it is not time-dependant. However, this observation gives us an important idea of sub-Nyquist rate sampling for system identification: nonlinear function $F(\ )$ of the system is not deteriorated regardless of the sampling rate of the input and output signal. Given a sufficient number of samples, $F(\ )$ can be characterized by most modeling methods in the

time domain, but methods dealing with signals in the frequency domain are not appropriate because of the aliasing [82].

To verify this idea, a simple hard limiter with QPSK signal input was characterized with different sampling frequencies, and its results are shown in Fig. 5.2. For the characterization of a simple hard-limiting device, three different sampling frequencies were used; one was at the Nyquist rate, and the other two were below the Nyquist rate. In particular, the signal bandwidth was 100 MHz, and the sampling rates were 23 MHz, 100 MHz, and 200 MHz. Notice that the characterization of the limiting function was successful for all three cases, although the numbers of sampled points were different during the specified period of sampling.

Contrarily, for the sampling of a nonlinear system with memory as shown in Fig. 5.3, this sampling-rate independency is not valid because the correlation between the current sampled input $x(n)$ and delayed input $x(n\text{-}k)$ becomes loose as the sampling rate is reduced, which means the loss of information about $F(\ )$. However, fortunately, systems with memory can be sampled with a moderately reduced rate based on the Generalized Sampling Theorem in the following section.

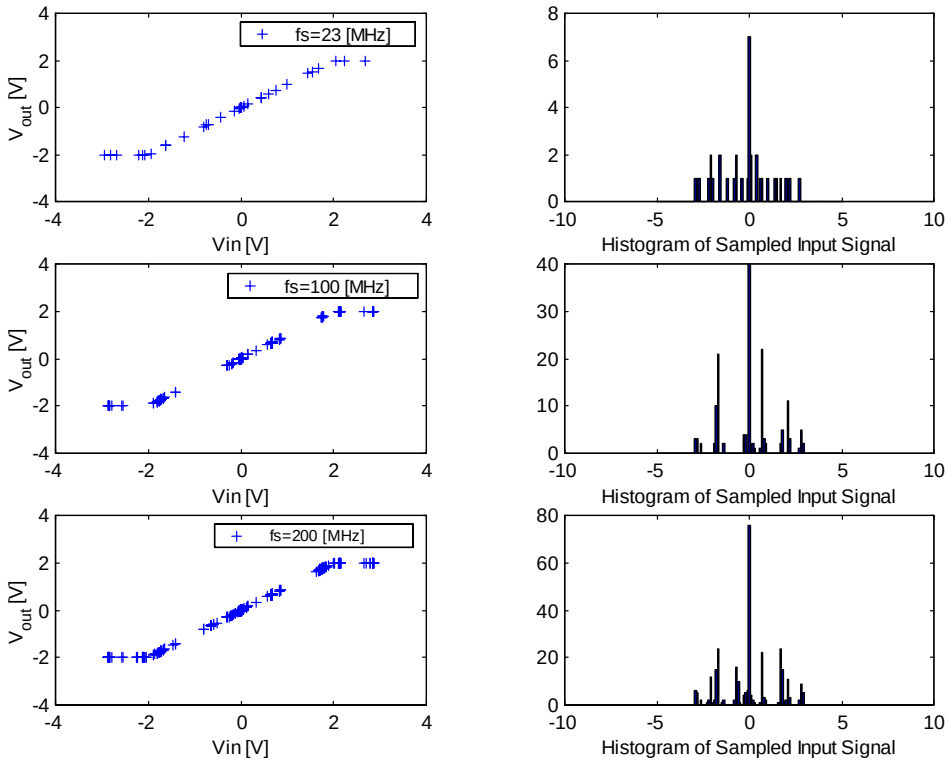


Fig. 5.2. Simulation results of the sub-Nyquist rate sampling of a limiter with QPSK signal of 100 MHz bandwidth.

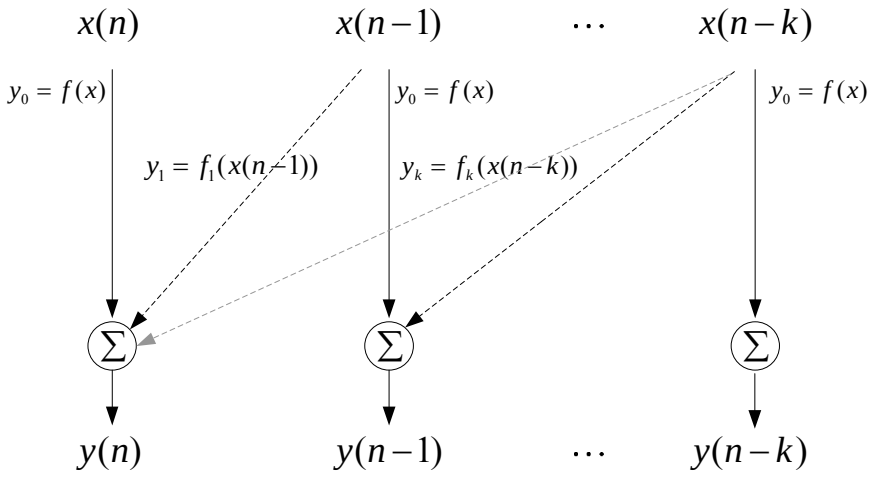


Fig. 5.3. Representation of a system with memory by input and output samples.

5.2.2 Zhu's Generalized Sampling Theorem

Assuming uniform sampling and that the signal is band-limited between f_h and f_l, the acceptable condition for sampling at a frequency f_s, without aliasing, can be expressed by

$$\frac{2 f_h}{k} \le f_s \le \frac{2 f_l}{k-1}, \tag{5.3}$$

where k is restricted to integer values that satisfy

$$2 \le k \le \frac{f_h}{f_h - f_l} \tag{5.4}$$

and

$$f_h \le 2 f_l \quad . \tag{5.5}$$

By sampling this way, the sampling rate can be reduced by k times. In terms of microwave system implementation, this harmonic sampling is useful not only because it enables us to sample a signal at a lower rate, but also it gives us the possibility of eliminating mixers in transceivers. Unfortunately, however, to guarantee alias-free reconstruction, this method still requires the A/D converter's sampling rate to be double the highest frequency component of the signal. Recently, Zhu and Frank individually published theories claiming that nonlinear systems, which often can be represented by Volterra systems, may be uniquely identified when the sampling rate is twice the input signal bandwidth [18], [83], [84]. Fig. 5.4 represents the concept for Zhu's Generalized Sampling Theorem used for the identification of a nonlinear system. It means that if the nonlinear one-to-one mapping function $g(\cdot)$ exists so that $g(y(t))$ is band limited, whether

$y(t)$ is band limited or not, then $y(t)$ can be sampled and uniquely determined at the Nyquist rate of $g(y(t))$, at the points $t_k = kT_s$.

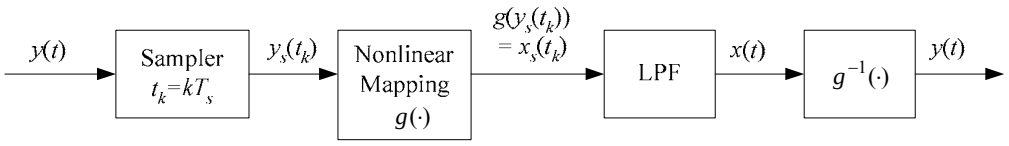


Fig. 5.4. Block diagram of Zhu's Generalized Sampling Theorem.

After Zhu's theorem, Tsimbinos *et al.* experimentally proved its validity by linearizing nonlinear devices for a single-tone signal based on the input Nyquist sampling rate [85]. Fig. 5.5 shows the application of the Generalized Sampling Theorem for system identification suggested by Tsimbinos.

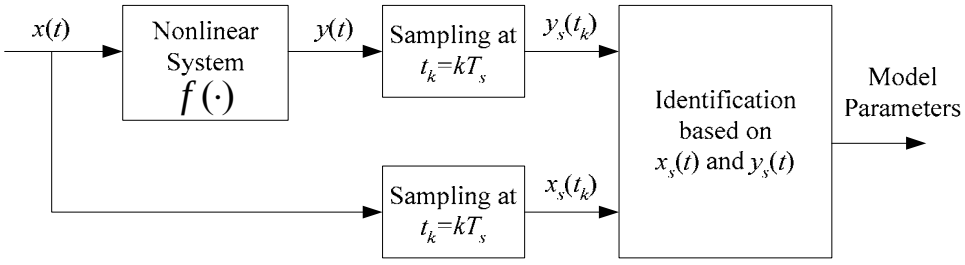


Fig. 5.5. Application of Zhu's Generalized Sampling Theorem for system identification.

On the other hand, Frank proved this concept with Volterra systems in the frequency domain. Assuming $x(t)$ is a band-limited signal, after passing this signal through a Volterra operator v^c, sample the output $y(t)$ with its Nyquist sampling rate, obtaining $y[n]$. Next, sample the input signal $x(t)$ and pass this through v^d, which is a discrete Volterra operator. Comparing the output of v^d with $y[n]$, he proved that the results are identical provided that v^c and v^d are consistent with each other. This concept can be expressed by a diagram, as in Fig. 5.6.

$$\begin{array}{ccc} x(t) & \overset{v^c}{\rightarrow} & y(t) \\ \updownarrow & & \downarrow \\ x[n] & \overset{v^d}{\rightarrow} & y[n] \end{array}$$

Fig. 5.6. Relationships of continuous and discrete-timed input and output signals through Volterra operators.

In conclusion, he claimed that the input and output signals sampled at the input Nyquist rate can be used to identify Volterra systems. In addition to this work, Martin showed that the generalized sampling theorem was applicable to any nonuniform sampling rates as long as the input Nyquist rate is preserved [86]. Tseng extended this generalized sampling theorem to identify cubically nonlinear systems [87].

5.2.3 Linearization of Nonlinear Devices from Subsampled Data

The under-sampling concept used so far is to sample bandpass signals (that have frequency components only between f_l and f_h) with a sampling frequency below the Nyquist rate [15], [16].

In case of a moderate nonlinear device, however, we suggest that it can be overlapped for the identification of nonlinearity of a PA, whereas the signal cannot be overlapped for the full reconstruction of the original signal (sub-Nyquist sampling). When a complex signal in the frequency domain is $S(f)$ at a frequency f_{IF}, and we sample it with f_s , the sampled signal in the frequency domain can be expressed with the series of $S(f)$ spaced by f_s, and with the series of $S^*(-f)$ spaced by f_s. If we say $S(f-f_{IF})$ is the frequency domain signal at the carrier frequency f_{IF}, the sampled signal is

$$S_{sampled}(f) = \sum_{n=-\infty}^{\infty} S(f - (n \cdot f_s + f_{IF})) + \sum_{n=-\infty}^{\infty} S^*(-f + (n \cdot f_s - f_{IF}))\,, \tag{5.6}$$

where n is an integer.

Since we're interested in signals at the lowest frequency for the A/D conversion, the signal of interest can be expressed as shown below:

$$S_{interest}(f) = [S(f - f_{IF}) + S^*(-f + (f_s - f_{IF}))]\,. \tag{5.7}$$

The original signal and its image signal start to overlap when $f_s = BW + 2^* f_{IF}$; if we put (5.7) into a bandpass filter designed to pass from $f_{IF} - BW/2$ up to ½ f_s, this is

suggested for use for the nonlinear characterization. Similarly, we can digitize the distorted signal at the output of PA and then compare both signals in the complex domain so that we can identify the AM/AM and AM/PM distortions of the PA. Fig. 5.7 shows the concept of this sampling. In terms of the lowest limit of this sub-Nyquist rate sampling theorem (we call this subsampling interchangeably from this point), it is expected to be the sampling limit of the input signal [85].

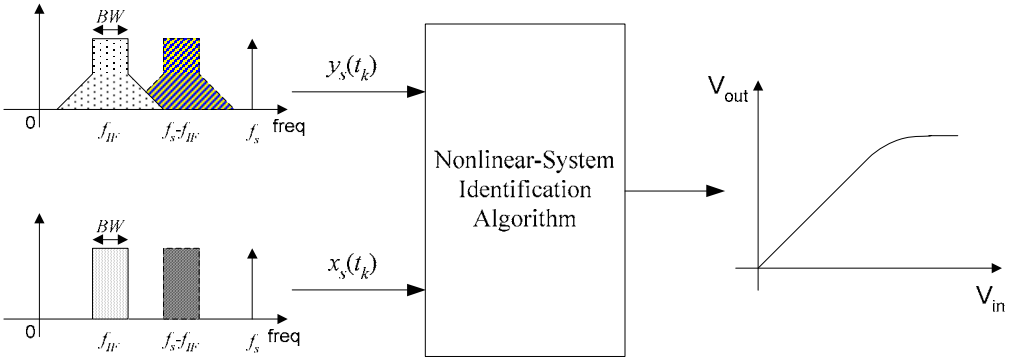


Fig. 5.7. Subsampling concept in the frequency domain.

This subsampling can be very handy when it comes to a wideband signal because we can still fully identify its characteristics even though a portion of the signal is folded, whereas the sampling frequency presumed so far must be at least six times its bandwidth if we include the third-order distortion. Thus, we do not need to decide the exact sampling frequency of a nonlinear device for its identification and this leads to the mitigation of the system requirements.

5.3 PA LINEARIZATION FROM SUBSAMPLED FEEDBACK SIGNALS

5.3.1 Predistortion Architecture

With data sets taken at the input and the output of a device, the indirect learning architecture is adopted for the predistortion, as proposed in Fig. 5.8. The main benefit of this architecture is achieved when we do not have any access to the original data to compare the output signal with. The second benefit is that it is not required to have additional processes to take the inverse of a device model because the direct generation of the predistortion function is sufficient.

Fig. 5.8 shows the architecture of an indirect learning architecture.

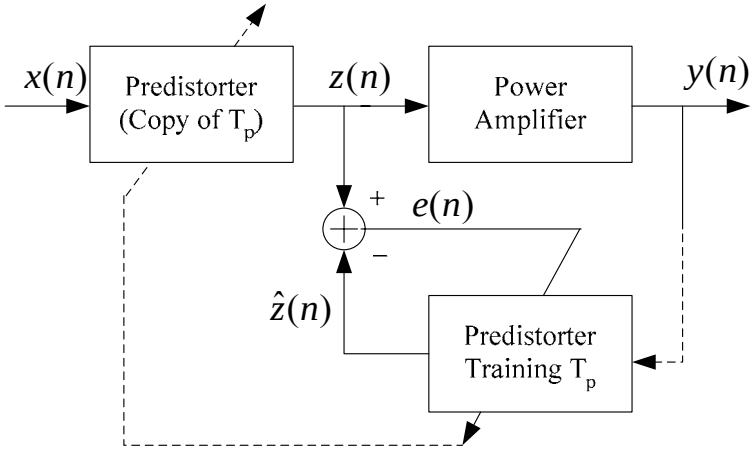


Fig. 5.8. The indirect learning architecture for the predistorter.

5.3.2 LUT Algorithm

In order to compensate for the time-varying property of a PA, the least mean square (LMS) method is used as the adaptive predistortion algorithm.

If we assume the sampled input and output signal of a PA as $z[n]$, and $y[n]$, respectively, the output-distorted signal can be expressed as

$$y[n] = G(z[n]) \cdot e^{j\Phi(z[n])}, \tag{5.8}$$

where $G(\cdot)$ and $\Phi(\cdot)$ are the PA amplitude and phase distortions, respectively. These $z[n]$ and $y[n]$ signals are used to generate an LUT for AM/AM and AM/PM compensation with LMS algorithm as below:

$$LUT\ (x[n+1]) = LUT\ (x[n]) + \mu \cdot x[n] \cdot e[n], \tag{5.9}$$

where μ is a stability factor and $e[n] = (z[n]\text{-LUT}(y[n]))$.

5.3.3 Simulations

In this section, we illustrate the AM/AM and AM/PM characterization of a PA with the suggested subsampling concept. A polynomial PA model for the Stanford Microwave's SHF-0189 (0.5W) was used for the simulation; the test signal was 1.2288 MHz IS-95B signal and the aperture width for the sample and hold circuit was 10 [nsec]. This PA is believed to have negligible memory effects. Fig. 5.9 and Fig. 5.10 are its characterization results in the time domain when f_s are 10 MHz and 5.3 MHz, respectively.

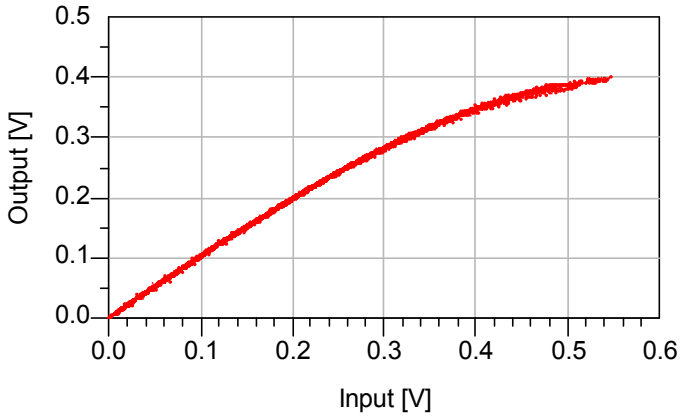


Fig. 5.9. Simulated AM/AM characteristic of SHF-0189 when fs = 10 MHz.

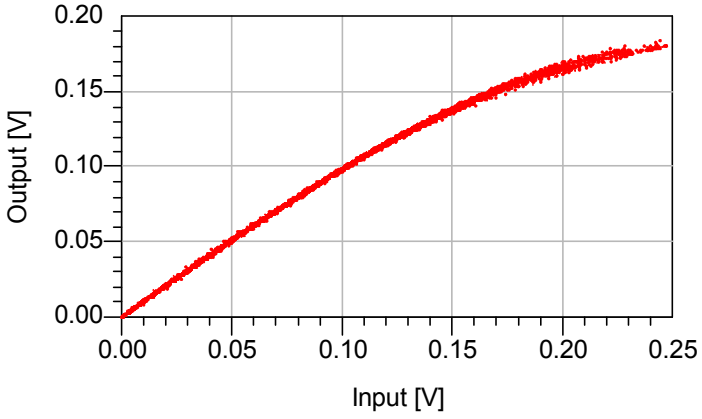


Fig. 5.10. Simulated AM/AM characteristic of SHF-0189 when fs = 5.3 MHz (where input spectrums are next to each other).

Fig. 5.11 and Fig. 5.12 show the spectrum with the same sampling frequencies, 10 MHz and 5.3 MHz, respectively. Particularly, Fig. 5.12 for 5.3 MHz of sampling shows that severe aliasing is taking place at the output spectrum, where the replicas of the input spectrum are adjacent to each other. The lower sampling frequency of 5.3 MHz was chosen because the input signal spectrum starts to overlap at this point.

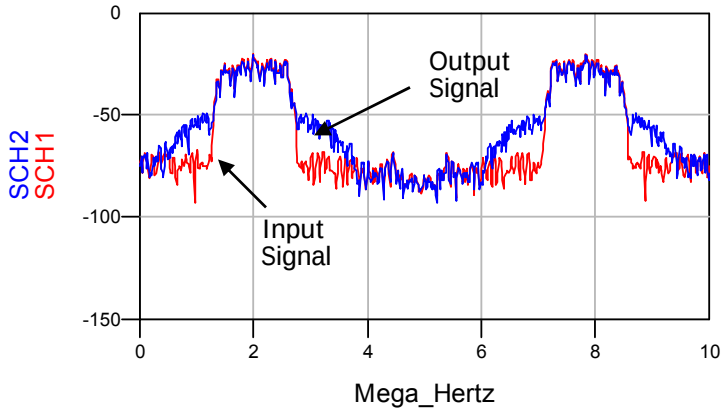


Fig. 5.11. Simulated spectrum of SHF-0189 with full Nyquist rate sampling, *f*s = 10 MHz.

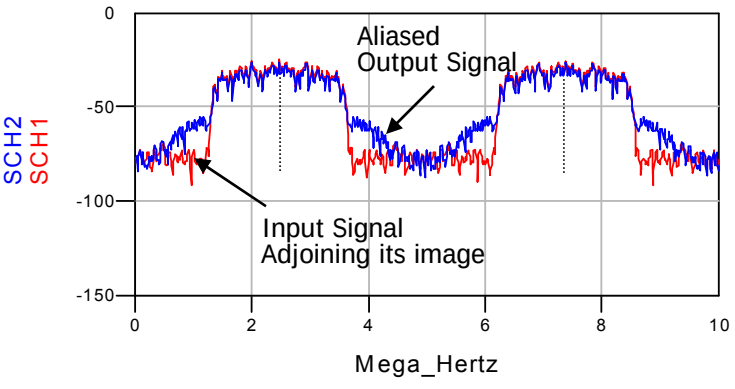


Fig. 5.12. Simulated spectrum of SHF-0189 with sub-Nyquist rate sampling, *f*s = 5.3 MHz.

Note that the nonlinear characteristics were clearly identified with f_s =10 MHz of sampling as well as with f_s =5.3 MHz, where the input spectrums are next to each other. In the definition of aliasing, measuring the amount of separation of input signals by the input bandwidth *BW* can be a figure-of-merit. Therefore, in Fig. 5.12, where the input signal adjoins its image signal, it can be called a 0% of *BW* separation. This situation can be also interpreted as having 67% of the output spectrum overlapped with the image signal.

The downside of the latter case is that there is a less chance of capturing the signal energy, but this can be overcome with a proper scale factor for the predistortion.

5.3.4 Measurements Setup and Results

To verify the subsampled predistortion architecture, we constructed a test-bed consisting of two sampling downconverters connected to the input and output of a PA, as shown in Fig. 5.13. The outputs of the downconverters were applied to a dual channel receiver and demodulated to calculate the PA distortion. The sampling rates of the downconverters were varied over several times of magnitude, and the receiver bandwidths were adjusted accordingly. We then adapted an LUT to optimally correct the baseband signals and thus predistort the PA.

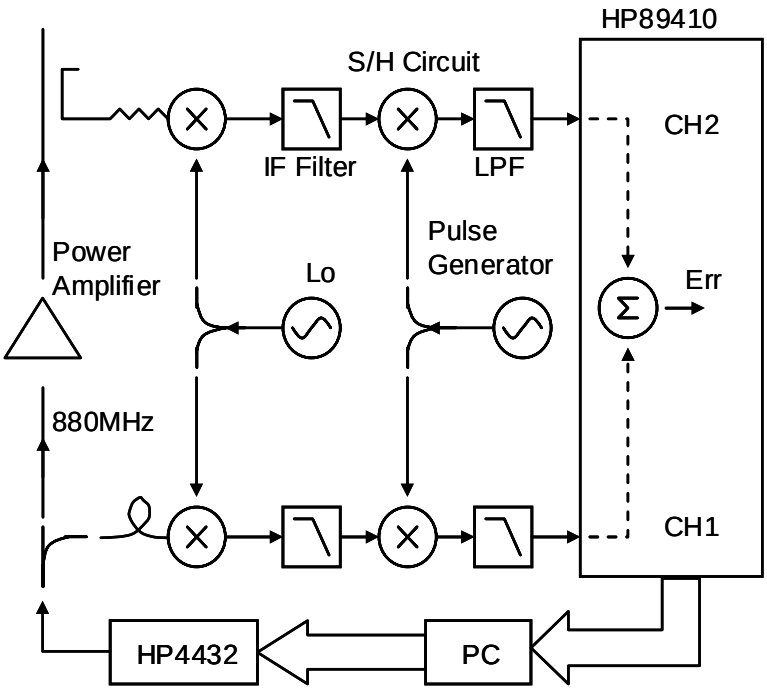


Fig. 5.13. Subsampling downconverter test-bed block diagram.

The measurement was done with an IS-95B signal at 880 MHz. The predistorted PA was 0.5W-Stanford Microwave's SHF-0189. Downconverted IF signals are captured using narrow aperture sample-and-hold circuits formed by wideband mixers and a pulse generator. These sampled signals are fed into the Vector-Signal- Analyzer (HP89410) where signals are digitized and then demodulated into IQ baseband signals. Hence, we can compare amplitudes "before" and "after" the PA even though they were aliased because of the low sampling frequency. A PC analyzes this information and generates an LUT that is used to predistort the baseband signals by complex multiplication.

AM/AM characteristics with f_s =10 MHz and f_s = 5.3 MHz were measured. The first case includes all the distortion information within its sampled frequency band, whereas the latter case has aliased third- and higher-order signals. The lower frequency f_s = 5.3

MHz was chosen because that frequency is where the adjacent "'input signal spectrums" start to overlap each other. This means 0% of *BW* separation as defined previously. The identification results after the narrow-aperture sample-and-hold circuits are shown in Fig. 5.14 and Fig. 5.15, respectively. From these graphs, we can see that the f_s =10 MHz case shows a clear AM/AM curve, and that f_s = 5.3 MHz case does, too, although it has a little bit of fuzziness owing to some cross-talk from the adjacent input signal spectrums.

The adjacent-channel power-ratio (ACPR) variation after predistortion is shown in Fig. 5.16 and is based on these identifications with different sampling rates. They were measured at 885 kHz offset, with 1.2288 MHz IS-95B signals. The number of samples collected at all sample rates was between 1,200 and 1,600 for each LUT iteration.

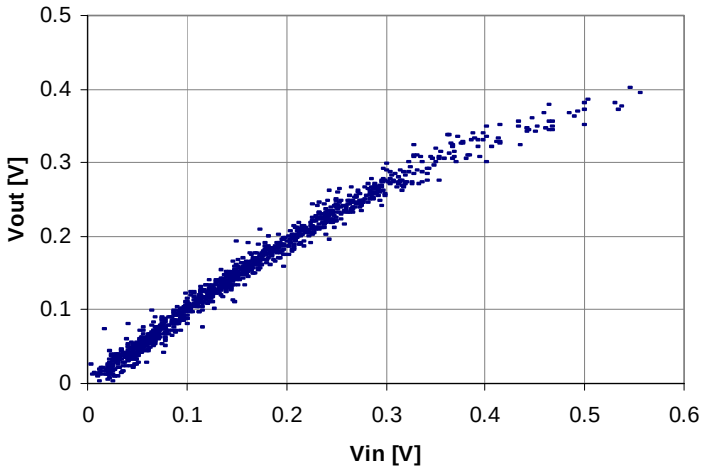


Fig. 5.14. Measured AM/AM characteristic of SHF-0189 when *f*s = 10 MHz (includes third-order distortions).

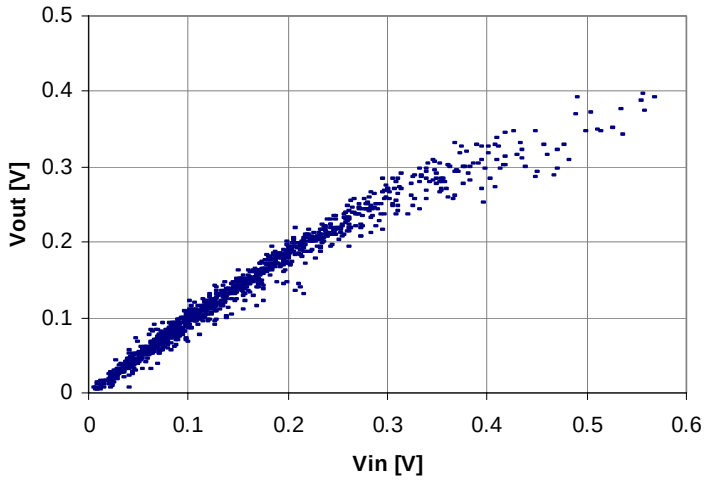


Fig. 5.15. Measured AM/AM characteristic of SHF-0189 when fs = 5.3 MHz (when input spectrums are next to each other).

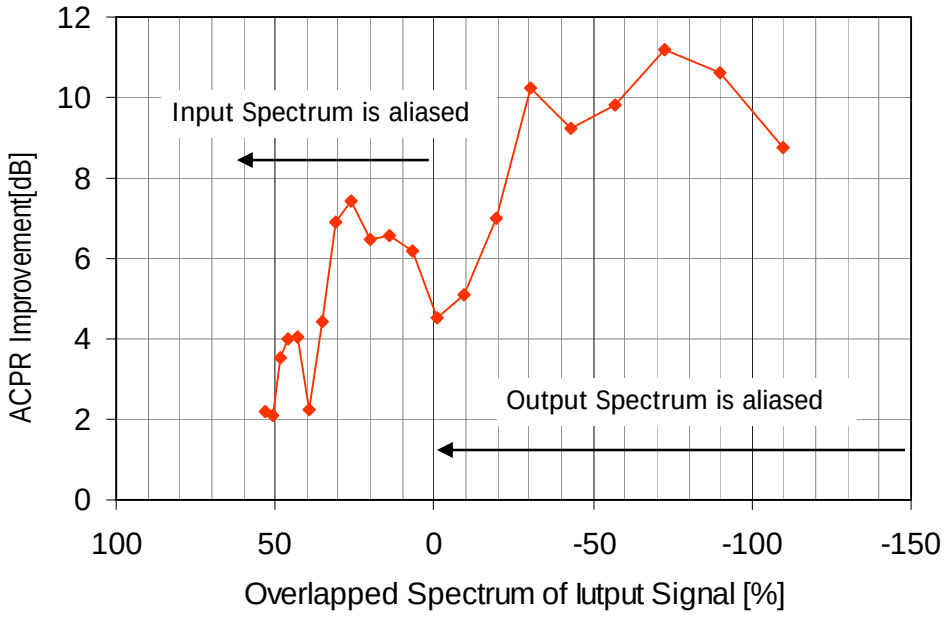


Fig. 5.16. ACPR improvement using subsampling predistortion architecture (Negative value in x-axis means that it is above the input Nyquist rate.)

The x-axis in this graph indicates the ratio of the overlapped spectrum to the output signal spectrum. The negative values in the x-axis mean that the input spectrum is not aliased; the output spectrum, which has wider bandwidth, might be aliased. It is clear that the performance of the predistorter was not affected by lower than output Nyquist-sampling rates until the input spectrums were off by -33% of *BW*. Below this value, the system identification performance begins to degrade. In this figure, a little bit of bounce in performance around f_s = 2~3 MHz (0 ~ 33% of overlapping region) is noticeable, and the reason for this is assumed to be the result of the bandpass sampling of the image signal between 0 and f_{IF} range, although this bandpass sampling was not intended. In this section, a sub-Nyquist rate sampling architecture for LUT generation in adaptive predistortion linearization systems has been developed. Its application to the predistortion of 0.5 W PA was successful, indicating 10 to 12 dB of ACPR improvement.

5.4 LINEARIZATION OF FREQUENCY MULTIPLIERS FROM SUBSAMPLED FEEDBACK

A Schottky-diode frequency tripler was designed and built for the output at 2.46 GHz with the input at 820 MHz. A complex modulated signal is generated in a PC and loaded into an Agilent E4432B arbitrary waveform signal generator; the upconverted RF signal was then applied to the device; the output signal from the device is downconverted to an IF and digitized through a digital oscilloscope. Then, the nonlinear characterization is processed in a PC, and the predistortion signal is generated and loaded

into the signal generator. By delicately changing the sampling period and IF frequency, we can control the sampling frequency and the amount of spectrum overlapped because of the subsampling. Fig. 5.17 represents the overall setup.

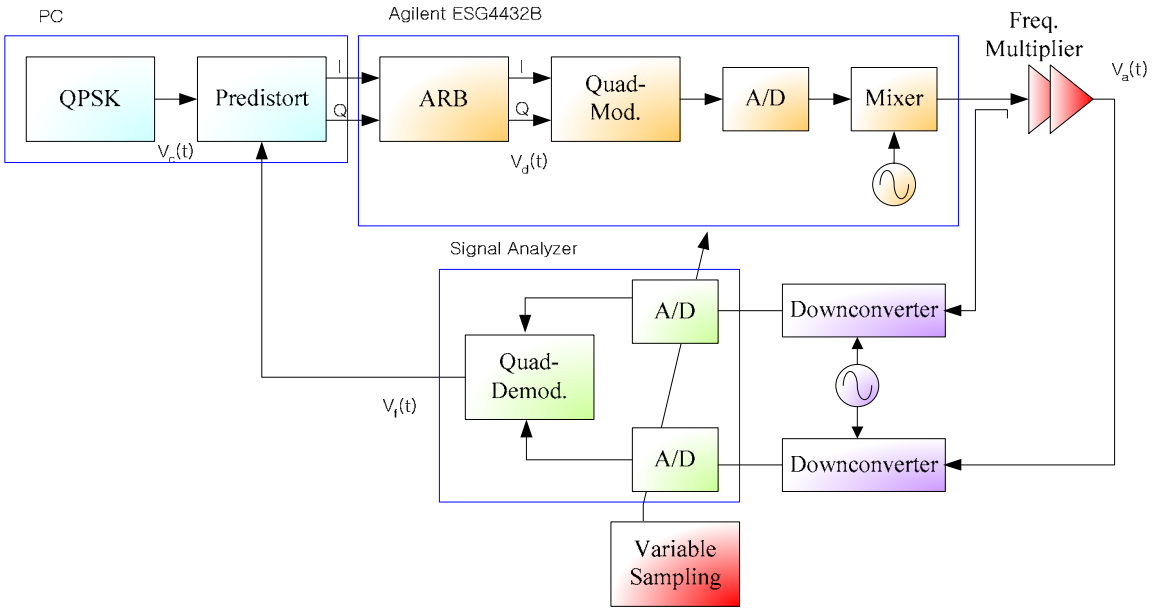
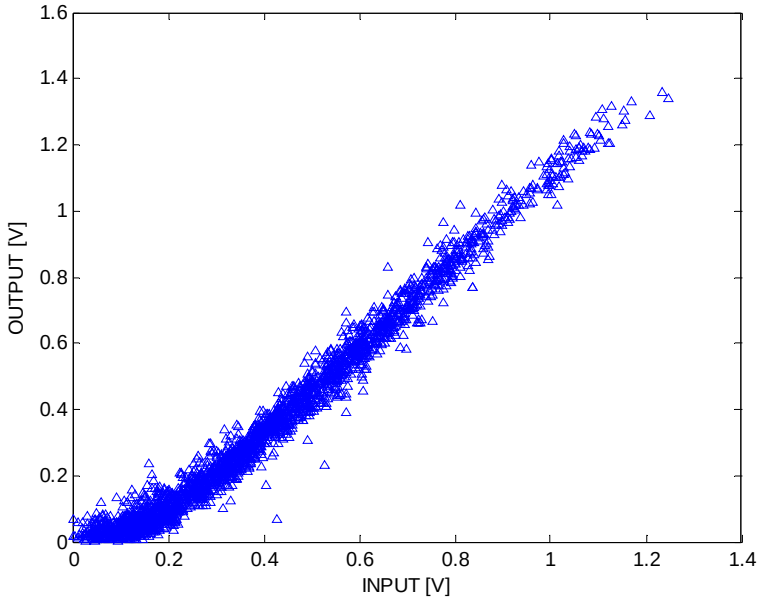


Fig. 5.17. Predistortion setup with variable sampling rate to linearize frequency multipliers.

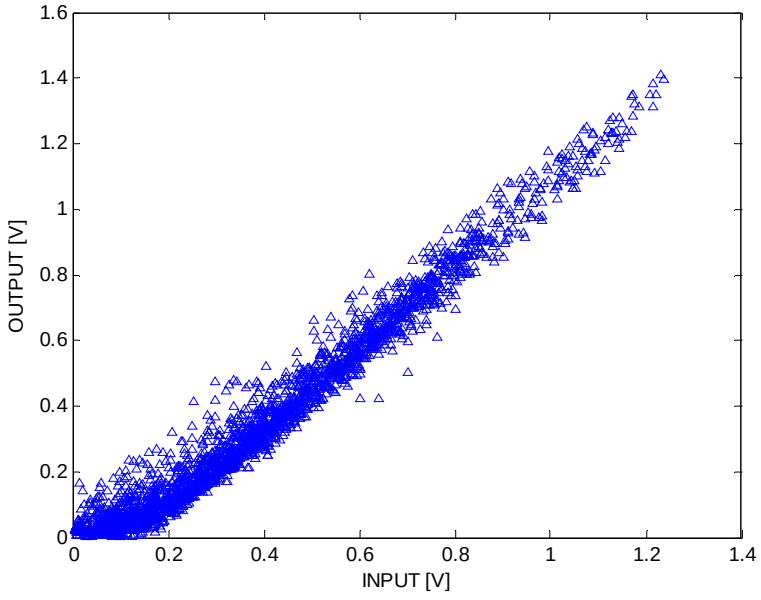
The performance of subsampling predistortion was evaluated by the ACPR marker reading at 885 kHz offset from 2.46 GHz. AM/AM characteristics measured with two different sampling ratios were shown in Fig. 5.18. The first graph shows the characteristics taken with the full sampling rate, and the second graph shows the result when -50% of the input spectrum is aliased, which means that the main output spectrums are off by 50% of *BW*. However, the third-order spectrum is still aliased because of the subsampling. For example, in Fig. 5.18 (a), we can say that output spectrums are off by

100% of *BW*. As can be seen from Fig. 5.18 (b), it is clear that subsampling the output signal can successfully characterize the frequency tripler.

Fig. 5.19 shows the output spectrums of an IS-95B signal at 2.46 GHz with full sampling. Note that without any predistortion, the spectrum is spread over three times the input spectrum, and its ACPR is just 3 dBc.

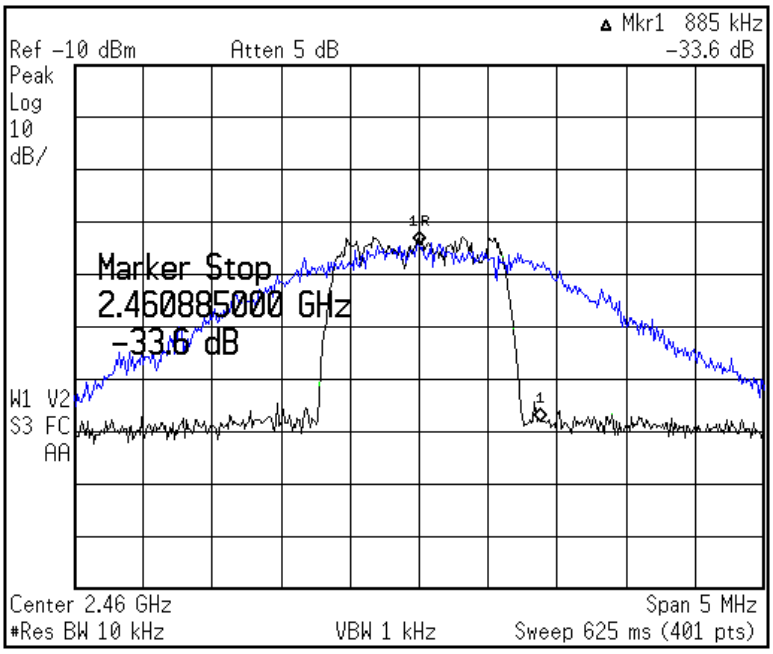


(a)

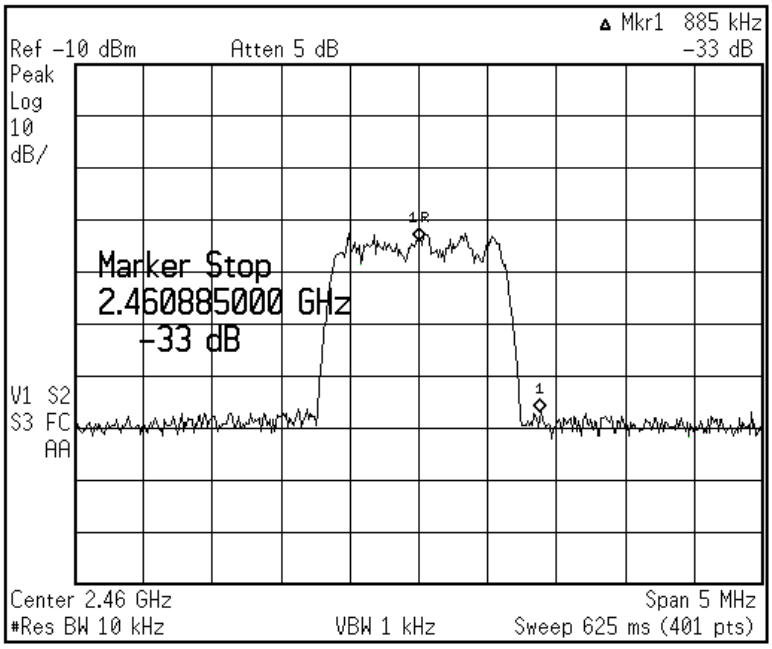


(b)

Fig. 5.18. Measured AM/AM characteristic of Schottky-diode frequency tripler sampled with: (a) above Nyquist rate (b) the rate at the third-order spectrum is overlapped by *BW* (-50% aliasing of input spectrum).



(a)



(b)

Fig. 5.19. Predistortion result of the frequency tripler. (a) Without any aliasing of sampled signal. (b) When the third-order spectrum is overlapped by *BW* (When -50% of input spectrum is aliased due to the subsampling.)

After the predistortion, the nonlinear characteristics were successfully corrected, taking the ACPR to 33 dBc, which was mainly limited by the dynamic range of the system.

The predistortion result with subsampled data is shown in Fig. 5.19 (b). From this graph, we can observe that the spectral overlapping from subsampling did not adversely affect the performance of the predistortion system. Fig. 5.20 shows the predistortion results with various amounts of spectrum overlap. The performance stayed the same and started to degrade around 0%, when the main spectrums start to overlap. The degradation of the performance from this point is mainly because of the loss of phase information coming from the IQ crossover in QPSK.

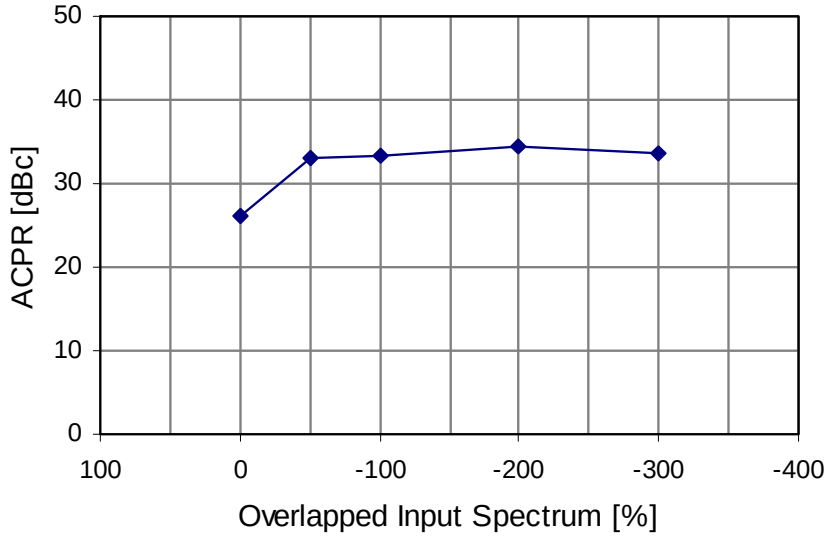


Fig. 5.20. ACPR Improvement using subsampling predistortion architecture (-100% in x-axis means that the main spectrums are off by 100% of input bandwidth, *BW*.)

In this section, a predistortion system with adjustable sampling frequency was implemented to linearize a Schottky-diode frequency tripler made by the author. Although subsampling causes aliasing of the signal spectrum, it can be used for the characterization and predistortion of a device without any loss of information. It was seen that sampling below the Nyquist rate of the output signal did not adversely affect the characterization of the frequency tripler. Based on the characterization, the AM/AM, AM/PM, and PM/PM distortion could be compensated for, verifying that frequency multipliers can be used as devices to translate complex modulated frequency signals to higher frequencies without distortion.

5.5 CONCLUSIONS

A sampling methodology for LUT generation in adaptive predistortion linearization systems has been developed. Using a narrow aperture sampling downconverter, samples of the envelope were obtained from input and output of the PA and a frequency tripler. It was seen that sampling below the Nyquist rate of the output signal did not adversely affect the correction capability of the algorithm. Ten to twelve dB of ACPR improvements were obtained for the predistortion of 0.5 W PA at sample rates down to 33% of the output Nyquist rate. In the frequency tripler case, the predistorter with various sampling frequencies achieved 33~34 dBc of ACPR until -50% of the output spectrum was aliased. Beyond this aliasing ratio, the demodulator starts to lose information, resulting in the ACPR of 26 dBc with 0% of input spectrum aliasing.

Consequently, we can conclude that subsampling the output spectrum can be applied to feedback paths in predistortion systems for PAs and frequency multipliers.

It was also empirically verified that the indirect learning architecture could be adapted to a predistortion system in which the original data fed into the predistorter is not accessible. Additionally, this characterization with the sub-Nyquist rate sampling concept might be extended to the subsampling downconversion, which takes advantage of the bandpass sampling of an aliased signal because of the subsampling at IF frequency. By doing so, we can reduce the A/D converter bandwidth requirements and may eliminate the need for a downconverting mixer, resulting in a low distortion system.

CHAPTER 6

SUMMARY AND FUTURE RESEARCH

The objective of this dissertation is the development of simplified reconfigurable transmission systems with digital predistortion of frequency multipliers to transmit complex modulated signals. For these applications, frequency multipliers are used as frequency up-converting devices for transmitted signals. The original contributions of this dissertation include the first development of frequency multiplier-based complex modulated transmission systems with digital predistortion; the first development of a zonal transfer function for the analysis of nonlinearity from frequency multiplication; the first development of reconfigurable dual-band active transmission systems, and the first verification of sub-Nyquist rate sampling in predistortion of complex modulated signal transmission.

Because a frequency multiplier has strong nonlinearities by nature, frequency multiplier-based transmission systems require proper linearization techniques and accurate modeling of the signal transfer function. Therefore, the characterization of distortion from frequency multipliers was first performed to generate an exact inverse

signal for predistortion. Based on this characterization, the expanded modulation transfer matrix was introduced to model the nonlinearity and generate the inverse function. It was revealed that in addition to the AM/AM and AM/PM distortion, PM/PM was the next major source of distortion for the transmission of digital signals.

Next, the predistortion system was verified by applying an IS-95B signal to various frequency multipliers built by the author, which include a Schottky-diode frequency tripler at 2.4 GHz, active dual-mode frequency doublers at 1.8 GHz, and varactor frequency doublers at 1.8 GHz. The output signals were successfully transmitted to the desired harmonics of fundamental frequencies.

Then, two methods for dual-band transmitters using frequency multipliers in conjunction with digital predistortion linearizers were developed to realize reconfigurable transmission systems with frequency multipliers. One method uses a circuit topology that can be switched between a fundamental-mode in-phase combined amplifier, and a push-push frequency doubler using input phasing. Investigation of circuit topologies to maximize output harmonics out of regular power amplifiers was performed, and a bi-tuned output combining technique was introduced for maximum output in amplifier-mode and doubler-mode operation. The second suggested method uses a fundamental-frequency power amplifier followed by a varactor multiplier that can be bypassed with an RF switch. Varactor-diode doublers with a minimal conversion loss were built and tested.

The last part of the dissertation investigates methods to minimize the requirements for A/D converters in a feedback network of the nonlinear identification system. Because the output signals at higher harmonic zones occupy wider frequency bandwidths than the

signal in the fundamental zone and thus make traditional sampling harder, a simplified but effective sampling method called sub-Nyquist sampling was developed. This sampling methodology was verified through the predistortion system of frequency multipliers and PAs, based on the sub-Nyquist rate sampled data.

Overall, this work will contribute to the development of low-cost and size-effective reconfigurable transmission systems because of the simplified architectures of transmitters and because of the relaxation of sampling requirements for the feedback networks.

Several topics for research related to this work suggest themselves. Two of the most important, because they are major challenges to the distortion-free transmission of digital signals in frequency multipliers, are (i) identification of the memory effect that occurs in frequency multipliers and (ii) development and implementation of a capability to cancel the operation of this memory effect on the predistortion system. The next research topic lies in investigation of ways to increase output dynamic ranges to accommodate signals of high PAPRs. This research might overcome the normally expected reductions of signal dynamic range that are part of the higher order transfer characteristics of frequency multiplication.

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